Consumer and Corporate Affairs Canada
Consommation et Corporations Canada

10/526510
DT5 Rec'd PCT/PTO 04 MAR 2005

(11) (A) No. 1 247 252

(45) ISSUED 881220

(52) CLASS 354-237
C.R. CL. 354-34

(51) INT. CL.[4] G07B 17/02

(19) (CA) **CANADIAN PATENT** (12)

(54) Electronic Postage Meter Having Non-Volatile Memory Selection Means

(72) DiGiulio, Peter C.;
Stalzer, Henry,
U.S.A.

(73) Granted to Pitney Bowes, Inc.
U.S.A.

(21) APPLICATION No. 503,779

(22) FILED 860311

(30) PRIORITY DATE U.S.A. (710,871) 850312

No. OF CLAIMS 4

Canada

DISTRIBUTED BY THE PATENT OFFICE, OTTAWA.
CCA-274 (11-82)

BEST AVAILABLE COPY

508779

ELECTRONIC POSTAGE METER HAVING NONVOLATILE MEMORY SELECTION MEANS

Abstract

An electronic postage meter having an improved memory selection circuit is disclosed. A custom memory map decoder circuit with resolution down to a single byte location is used to provide selection enabling signals to insure the selection of an appropriate device only when the addresses appropriate to that device are communicated. In accordance with the invention, at least two nonvolatile memories are provided. Writing to either of these nonvolatile memories is inhibited unless one and only one memory is selected. The circuit also prevents the selection of either of the nonvolatile memories in the event that the write strobe signal to the memories is held active.

ELECTRONIC POSTAGE METER HAVING A NONVOLATILE MEMORY SELECTION MEANS

The invention relates to postage meters and in particular to electronic postage meters having microcomputer control of printing and accounting functions.

Devices of this type are generally known, and are discussed for example in U.S. Patent No. 3,978,457. This patent discloses a system for a postage meter which includes a keyboard for the manual introduction of data corresponding to the postage to be printed in a Random Access Memory for real time operation. Data is stored in a nonvolatile memory upon power down and read into the Random Access Memory upon power up.

U.S. Patent No. 4,481,604 describes an electronic postage meter having a redundant memory system in which for each postal printing operation identical data is stored, respectively, in two separate but identical CMOS battery-backed nonvolatile memories.

In these known devices, there have been found to be times when essential data has not properly been stored in the nonvolatile memory of the meter. It has been found that one reason might be the improper selection of access to a particular device.

In known electronic postage meters, the microprocessor high order address bits or combination thereof are utilized in a standard decoder for selecting or enabling a particular

memory or peripheral device to be accessed in accordance with the microcomputer instructions. While this normally works well, in many cases of improper operation of the microcomputer or failure of one of the address lines of the bus, an improper bit may be decoded and the select logic gate which then enables the wrong device may cause wrong data to be read from memory or in the worst case cause data to be written into an unknown memory or peripheral with no indication of any malfunction. When this happens there is a strong possibility of service personnel's not being able to recover essential information from the nonvolatile memory in the postage meter when the postage meter fails.

In accordance with the invention, at least two nonvolatile memories are provided. In order to assure that data is written only to a selected nonvolatile memory, a logic circuit is provided which will decode the addresses called by the microprocessor to select one of these Nonvolatile Memories and which will enable a write strobe signal from the microprocessor to communicate with the NVM only when one and only one memory is selected. The logic circuit also includes means for preventing the selection of either of the nonvolatile memories in the event that the write-strobe signal is held active.

It is accordingly an object of an aspect of the invention to provide a write strobe signal to the nonvolatile memory only when the appropriate addresses are communicated from the microprocessor so as to particularly insure the reading and

writing of the appropriate data into the appropriate location.

It is an object of an aspect of the invention to provide in an electronic postage meter a means for assuring that the information in nonvolatile memory may be altered only upon further verification that such altering is intended.

It is an object of an aspect of the invention to prevent the writing of information to Nonvolatile Memory under circumstances where such writing would at all times be enabled due to a malfunction in the Electronic Postage Meter.

An aspect of the invention is as follows:

In a postage meter having a mircroprocessor for controlling the printing of value and for accounting for the printing of such value and at least two nonvolatile memories for storing information, said microprocessors being operative to read ~~information from and write information to said nonvolatile~~ memories, said microprocessor providing a write strobe signal operative for enabling writing of information into said nonvolatile memories, nonvolatile memory selection means comprising a logic circuit for selecting one of said nonvolatile memories in accordance with information from the microprocessor, and means for blocking said write strobe signal to said nonvolatile memories when neither of said nonvolatile memories is selected.

Other features and objects of the invention will become apparent in conjunction with the description of the drawing wherein:

FIG. 1 is a block diagram of an electronic postage meter in accordance with the invention;

FIG. 2 is a block diagram of a specific arrangement of a processor interface circuit in accordance with the invention;

FIG. 3 is a schematic of a decoder arrangement in accordance with the invention;

FIG. 4 is a default memory map showing a preferred arrangement of memory locations in accordance with the invention;

FIG. 5 is an embodiment of a circuit for providing a plurality of control output signals for NVM access;

FIG. 6 shows a preferred embodiment for providing a signal in response to an illegal address selection;

FIG. 7 shows in schematic form a preferred embodiment of a circuit for providing NVM selection;

FIG. 8 shows in schematic form a status and control circuit arrangement;

FIG. 9 is a schematic of a circuit for control of interrupts to the system microprocessor;

FIG. 10 is a timing diagram of the events; and FIG. 11 is a timing diagram.

Referring now to FIG. 1 which is a block diagram of a meter in which the invention may be incorporated. Such meters are known and are described for instance in U.S. Patent No. 3,978,457 to Check, et al and assigned to the assignee of the present invention. In this patent, the working memory under control of the CPU is a Random Access Memory from which data must be transferred to a nonvolatile memory upon loss or shutdown of power to the meter.

U.S. Patent No. 4,481,604 assigned to Roneo Alcatel discloses an electronic postage meter where the Random Access Memory and the nonvolatile storage memories are combined in battery backed CMOS RAMs which are used both for the real time operation and for long term storage of information in postal registers. EPC Application No. 0 085 385 published August 10, 1983, and assigned to the assignee of the present invention discloses an improved dual non-memory system. It will be appreciated by those skilled in the art that such a device may be combined with the electronic postage meter described in Check and is also suitable for the invention disclosed herein. The decoder arrangement disclosed herein is conveniently used to provide a method and apparatus for further protecting essential postal data in conjunction with the circuit described in Canadian Application Serial No. 503,785 filed on even date herewith entitled POSTAGE METER WITH A NONVOLATILE MEMORY PROTECTION CIRCUIT and assigned to the assignee of the present invention.

Still referring to FIG. 1, the heart of the general functional arrangement of the system is the CPU which is utilized with specific instructions programmed in the Read Only Memory (PM), for the performance of control of the basic meter functions, for the performance of calculations based on any input data and for controlling the flow of data into the various memories.

The system, may operate in accordance with data applied from an appropriate input means "I" or from a communications means "C" such as described for instance in U.S. Patent No. 4,301,507 to Soderberg. The data is fed into the CPU under control of the program in Read Only Memory and at any time during the operation of the system, should the contents of the memory storing the appropriate credit/debit balances or other cumulations in accordance with various features of the system be desired to be displayed, appropriate instructions provided by the input means "I" cause the CPU to access the desired locations in memory which store the information requested.

The information may be displayed on an output unit "O". As well known, the input and output units may be multiplexed by a suitable multiplex unit "MP" for transferring data to and from the CPU.

FIG. 2 is a block diagram of a specific arrangement of a processor interface circuit in accordance with the invention and comprises an address decoder and associated selection circuitry for the selection and control of various elements of the Electronic Postage Meter. It will be appreciated that the circuit arrangement herein described is preferably embodied in a custom LSI microchip, however, it will be understood that the use of conventional logic components is also contemplated.

Turning now to FIG. 2, the overall block diagram of the circuit is shown generally at 10. The demultiplexer 12 in conventional manner demultiplexes the address/data bus 14 of a microprocessor (not shown in FIG. 2), suitably an 8085 series microprocessor available from the Intel Corporation or an NSC800 series microprocessor available from the National Semiconductor Corporation. The bus 14 communicates with the demultiplexer 12 on communication lines 16 through a conventional transceiver circuit arrangement 18. For best results the ADDRESS LATCH ENABLE (ALE) signal 20 from the microprocessor is "anded" with the microprocessor read strobe signal 22 to provide the latching signal for latching the address information for the demultiplexer 12.

The demultiplexed address information is fed out on lines 24 for use in other parts of the EPM and are internally

connected at 26 to the decoder section 28. The high order address signals directly from the microprocessor are communicated on lines 30 to the decoder section 26. An external decode signal, $\overline{\text{EXTDEC}}$, is also input to the decoder section 28.

The decoder section 28 receives and decodes a complete input address received at 26 and 30 to provide select outputs for the various parts of the system. The low order demultiplexed address lines AØ, Al and A2 are utilized as inputs to control flip-flops 32 along with the microprocessor write strobe $\overline{\text{WR}}$ received at 34 from the microprocessor. As described further below, the control flip-flop section generates four control signals in response to these inputs in addition to a decoder reset signal and other derived signals, i.e. EXT-INTP, a pulse signal generated at the activation of the illegal memory access output pin, and a select signal CONTRL-s for the selection of the Control Flip Flop block.

Outputs from the decoder 28 are provided to NVM output control block 36. This control block 36 in accordance with the invention provides a fail-safe NVM device selection. The selection of either NVM is disabled if the NVM write line is shorted to the "active" state. The NVM write strobe is disabled whenever the other devices are selected or in the event that both NVMs are simultaneously selected.

In accordance with the invention, an illegal address control block 38, in conjunction with the decoder 28 detects when the microprocessor read or write strobes attempt to access addresses an illegal, i.e. unused, memory space and,

as discussed below, provides a signal output for interrupting the processor.

Status and control block 40 monitors the outputs from the control Flip-Flop section and provides a control port to generate a decoder reset and to control the selection of an internal or external communication through an "Echoplex" I/O section 42. Preferably the section also includes an 8-bit timer to set the Transmit Baud rate for the serial communications.

Dual Timer section 44 provides two programmable 16-bit timers. Preferably the system clock is the clock input to the timers. Suitably each is programmable for continuous or for one-shot operation for generating an interrupt when the programmed count is completed. Conveniently an 8-bit counter divider can be selected to prescale the clock input or the ripple output of the first timer may be selected as the clock input to the second timer.

Conveniently serial I/O block 46 and parallel I/O block 48 are utilized for communication with a keyboard and display and for motor control, sensing postal value and miscellaneous control functions.

For best results, an Interrupt Status and Control Block 50 is provided along with an interrupt mask control port for enabling selected interrupts to interrupt the systems processor.

FIG. 3 shows a schematic of an embodiment of a decoder block for providing a decoded memory map in accordance with the invention. The crossed lines with a circle superposed

are used to indicate the preferred conductive path in a customized chip arrangement. It will be appreciated that the illustrated arrangement is extremely convenient in that the decoded memory map as described below may be modified easily with only a few mask changes.

The various addresses communicated in known manner from the microprocessor and demultiplexer as described previously are each fed to leads A1 through A15 of the decoder block 28. The address bits on address lines A11 through A15 are supplied to NAND gates 52, 54, 56, 58, and 60 and inverted at inverters 62, 64, 66, 68, and 70 and applied as illustrated to the NAND gates 52, 54, 56, and 58. An external decode signal 72 (see also FIG. 2) is applied to NAND gate 60. The output of NAND gate 60 is NOR'D with the outputs of gates 52, 54, and 56. The EXTDEC signal is also applied directed to gate 58. It will be noted that when "active" this signal will disable the decode function. The decoded outputs from the connections illustrated in FIG. 3 for the preferred embodiment are as shown in Table I and in FIG. 4.

TABLE I

OUTPUTS

ROM#	: SELECT FOR EXTERNAL PROM MEMORY
RAM#	: SELECT FOR EXTERNAL RAM MEMORY
SEL1	: FOR GENERATING THE SELECT FOR EXTERNAL NVM#1
SEL2	: FOR GENERATING THE SELECT FOR EXTERNAL NVM#2
CNTRL-S\	: SELECT FOR INTERNAL CONTROL FLIP-FLOP BLOCK
INTR-S\	: SELECT FOR INTERNAL INTERRUPT CONTROLLER
STAT-S\	: SELECT FOR INTERNAL STATUS BLOCK
TIMER-S\	: SELECT FOR INTERNAL DUAL-TIMER BLOCK
ECHO-S\	: SELECT FOR INTERNAL ECHOPLEX BLOCK
SERIAL-S\	: SELECT FOR INTERNAL SERIAL I/O BLOCK
PARALLEL-S\	: SELECT FOR INTERNAL PARALLEL I/O BLOCK
ECHO/VOID#\	: SELECT FOR EXTERNAL ECHOPLEX BLOCK OR SPARE DECODE SIGNAL WHEN UNUSED MEMORY SPACE IS SELECTED (OR NEITHER)
IO\	: ACTIVE WHEN ANY I/O SELECTS ARE ACTIVE
IOREAD\	: ACTIVE WHEN ANY OF THE INTERNAL SELECTS ARE ACTIVE
DVOID	: ACTIVE WHEN "ExtDec\" IS INACTIVE AND WHEN NONE OF THE SELECT OUTPUTS ARE ACTIVE

OUTPUT SIGNAL	ADDRESS RANGE(S)	SIZE
ROM#	ØØØØ - 7FFF	32 KBYTES
RAM#	CØØØ - C7FF	2 KBYTES
SEL1	DØØØ - D7FF	2 KBYTES
SEL2	EØØØ - E7FF	2 KBYTES
ECHO-S\	FFD8 - FFDF	8 BYTES
STAT-S\	FFEØ - FFE1	2 BYTES
INTR-S\	FFE2 - FFE7	6 BYTES
PARALLEL-S\	FFE8 - FFEB	4 BYTES
SERIAL-S\	FFEC - FFEF	4 BYTES
TIMER-S\	FFFØ - FFF7	8 BYTES
CNTRL-S\	FFF8 - FFFF	8 BYTES
IO\	FFD8 - FFFF	48 BYTES
IOREAD\	FFD8 - FFFF; IF "EXTECHO\" INACTIVE FFEØ - FFFF; IF "EXTECHO\" ACTIVE	

It will be noted that in accordance with the invention, an active DVOID output is provided from NAND gate 74 when none of the system's blocks are selected. It will also be clear to one skilled in the art that the address bits, when appropriately decoded as in the illustrated circuit by NAND gates 76, 78, 80, 82, 84, and 86 and inverters 88, 90,

92, 94, and 96 provide an "active" output IO whenever any of the I/O functions is selected and an "active" I/O read output whenever any of the internal circuit functional blocks are selected. Address bits A3 and A4 are applied to 2-to-4 demultiplexer 98 and decoded with other low order address bits for providing output signals as defined in Table I for selecting the appropriate blocks.

It will be understood that the signal DVOID is not necessarily limited to its previously described function. For instance, in the illustrated embodiment, a signal VINT from the control flip-flop block further described below may be used to convert this DVOID signal to another decode output. This signal shown as "ECHO/VOID" in FIG. 3 is available if the circuits internal ECHOPLEX block 42 is utilized. Alternatively it will be seen that if an external "echoplex" section is utilized, that is, when the signal "EXTECHO" is "active" the "ECHO/VOID#" output becomes the "select" signal for the external block and the "select" signal for the internal echoplex section, "ECHO-S" is disabled.

As mentioned previously, the Control Flip-Flop section 32, more particularly shown in FIG. 5, generates four control output signals and their complements for controlling the generation of an illegal address interrupt signal to the processor, to provide an independent enable/disable for the access to two separate NVM storage devices, to enable and disable meter postage printing and access to nonvolatile storage.

As best seen in FIG. 5 the low order address signals A0, A1, and A2 are fed to a 3-to-8 Line Decoder Multiplexer 102 equivalent to a 74HC138 available from RCA to set and reset flip-flops 104, 106, 108, and 110. The processor strobe signal $\overline{WR}$ and the select signal $\overline{CNTRL-S}$ are applied to the enable inputs of decoder 102. As illustrated, it is apparent that the control flip-flops are selectively controlled when both these signals are "active".

The decoder reset signal $\overline{RST}$ and $\overline{EXT-INTP}$ (a pulse signal generated at the activation of the illegal memory access interrupt signal) are "NAND'D" at "NAND" gate 112, inverted at inverter and applied to each of the flip-flops 104 and 110. Table II shows the preferred decoded control signals in response to the appropriate addresses.

TABLE II

AØ-2	DECODED CNTRL	FLIP-FLOP	OUTPUT	
Ø	VINT-CLR\	VINT	INACTIVE	
1	VINT-EN\	VINT	ACTIVE	PRESET
2	WR2-RESET\	WR2-EN	INACTIVE	PRESET
3	WR2-SET\	WR2-EN	ACTIVE	
4	WR1-RESET\	WR1-EN	INACTIVE	PRESET
5	WR1-SET\	WR1-EN	ACTIVE	
6	UNLOCK-SET\	UNLOCK	ACTIVE	
7	UNLOCK-CLR\	UNLOCK	INACTIVE	PRESET

The outputs from flip-flop 104 designated UNLOCK are preferably active to enable postage printing and for NVM access. For best results, the preset value is inactive to prevent printing and NVM access. The signal WR1-EN and WR2-EN are "active" for write access to respective NVM devices #1

and #2. Again, for best results the preset values are "inactive".

The output VINT which as previously discussed is fed to the decoder section 28 is active to enable an interrupt generation whenever an illegal memory access is attempted. It will be appreciated that this is preferred since in the "inactive" state it may be used to reset the generated interrupt signal or to disable the interrupt so that it may be used as a spare decode output. The VINT preset signal is "active" to enable the interrupt.

The illegal address control block 38 is shown more particularly in FIG. 6. This circuit is used to provide an indication of when access to unused memory space is attempted.

The $\overline{\text{DVOID}}$ decoded signal output from the decoder section 28 is nanded at NAND gate 106 with the $\overline{Q}$ output from a D Flip-Flop 108. The processors read strobe $\overline{\text{RD}}$ and write strobe $\overline{\text{WR}}$ are NAND'D at NAND gate 110, inverted and applied to the clock input of the D flip-flop 108. The decoder reset signal is NANDED with the "VINT" signal from the control flip-flop section 32 at NAND gate 112 and applied to the RESET input shown as $\overline{\text{CLR}}$ in the Figure.

Thus, depending upon the status of the signal VINT as discussed previously, the decoded void memory space indication will be latched at the lead edge of either the read or the write strobe of the microprocessor to provide the output INT-VOID from the Q terminal of flip-flop 108. In accordance with the invention, the INT-VOID signal is

provided to the system microprocessor as an interrupt signal. Preferably this indication will remain latched until reset by the reset signal from the microprocessor.

Conveniently as seen in FIG. 2 the output is inverted at inverter 116 and supplied at 118 at $\overline{\text{INT-VOID}}$.

For best results, this $\overline{\text{INT-VOID}}$ output pin in open-drain so as to permit any of a number of open-drain outputs wire-ored to this pin to activate the output signal. This output pin is then suitably tapped as the input signal $\overline{\text{EXT-INT}}$ which is furnished to the Status and Control Block. There, this signal is provided as a status port bit and upon its actuation, a 1 clock period pulse is generated on signal $\overline{\text{EXT-INTP}}$. This $\overline{\text{EXT-INTP}}$ is provided from the status and control section to reset the control flip-flop and parallel I/O sections to their default (safe) states when the $\overline{\text{INT-VOID}}$ output pin is activated.

Turning now the FIG. 7, the NVM Output Control Block 36 is shown in greater detail. In order to insure secure accounting in the NVM the WRITE access to the two independent NVM devices is independently enabled and disabled under software control.

The NVM OUTPUT CONTROL will block the microprocessor write strobe WR unless either of the NVM decoded select signals SEL1 and SEL2 is available and the appropriate write enable signal from the control flip-flops are available at NAND gates 118 and 120. The output of these gates are inputs to NAND gate 122 whose output is applied to NAND gate 124.

The output of this gate is inverted and supplied to NAND gate 126.

The other signals applied to NAND gate 124 are the decoded select signals NVM1, NVM2, ROM, RAM and VOID are taken from the output drivers and applied to NAND gate 124, with NVM 1 and NVM2 being NOR'D at NOR gate 128 and inverted before being applied to 124. It will be appreciated that the write strobe WR is blocked if the appropriate memory space is not selected. It will also be appreciated that if both NVMs are selected simultaneously the write strobe will also be blocked.

A further protection feature is provided in the event that the NVM write strobe output is shorted "active". The address enable strobe at 20 is applied as the clock signal to a D flip-flop 130. If the $\overline{\text{NVMWR}}$ is shorted active, the ALE signal clocks the Q output low to block both of the NVM device selection signals at NAND gates 132 and 134.

FIG. 8 is a schematic of the status and control block. The block comprises a status port to allow monitoring of the control flip-flop outputs. The outputs of the control flip-flop block 32 are applied to buffer 136 for output to data bus 138, see also FIG. 2. The system clock input from 140 (see FIG. 2) is used in conventional fashion for timing the internal reset output by counting through D flip-flops 142, 144, and 146 to provide signal IRST which is the control signal for resetting all of the flip-flops in the circuit and is applied along with the System Reset to AND gate 148, (see FIG. 2).

The block select signal $\overline{\text{STAT-S}}$ for this block, the write strobe, read strobe, and lowest order address bit are decoded to clock the writing of data at octal flip-flop 150, for initiating a general decoder reset under the control of appropriate software commands and for setting a baud-rate divider circuit if desired. The $\overline{\text{EXTECHO}}$ signal from D flip-flop 152 is used as previously discussed for selection of an external communication device (not shown).

The Interrupt Controller block 50 is shown in more detail in FIG. 9. The interrupt controller in accordance with the invention provides great flexibility in the servicing of the various interrupt signals to the microprocessor. The signal INT-VOID from the illegal address control block 38, signals INT-TO and INT-TI generated by the time-out of timers in timer block 44, signal INT-ECHO from the ECHOPLEX block 42 which is "active" to indicate the start of an echoplex message, signal INT-SERIAL from serial I/O block 46 which is "active" when new data is received or when the port is read for sending data, and signal INT-MOTOR from PARALLEL I/O block 48 which is preferably "active" when an illegal motor control output has been communicated are each input to the INTERRUPT CONTROLLER block 50. The status of each of these signals may be read out directly from buffer 154 when the $\overline{\text{RD-INTR}}$ signal is "active".

Signal $\overline{\text{INTA}}$ from the system microprocessor is an interrupt acknowledge. It will be appreciated that if the INTA line is held or tied in the "inactive" state, each interrupt signal input applied through gates indicated

generally at 156 and fed to NAND gate 158 will create an interrupt request signal $\overline{\text{INTR}}$ for communication to the system's microprocessor. Preferably, mask bits may be fed as data on data input bus 16 for providing masking bits to D-flip-flops 160 for latching. The latched outputs from 160 are applied to gates 156 so that the interrupt request will be generated whenever an unmasked device requests service. The particular device requesting service may be determined by reading the status buffer 154. The interrupt lines are also coded at the gates indicated generally at 162 for feeding to latch 164 which also provides similar information.

Preferably, as shown, there is also included a vectored interrupt for the handling of service requests. As discussed previously, a non-masked interrupt results in the generation of an interrupt-request signal to the systems microprocessor. For best results, the microprocessor upon receiving this signal will transmit an interrupt acknowledge signal $\overline{\text{INTA}}$. This signal places the contents of the opcode latch 166 onto the data bus. In accordance with the invention, the processor interprets this data as an opcode, normally a call instruction for the microprocessor. Upon execution of the instruction, the microprocessor generates another $\overline{\text{INTA}}$ pulse to enable the lower vector latch 168. The encoding of bits on this latch as described above. The vector thus generated, desirably reflects a predetermined code representing the highest priority interrupt. The next $\overline{\text{INTA}}$ pulse, in response to the call of this OPCODE, will

place the data residing in latch 170, preferably the upper vector address data, onto the data bus 138.

The $\overline{\text{INTR-S}}$ signal is utilized to select this block. The low order address signals AØ through A2 are used as illustrated to decode the various control signals on the gates indicated generally at 140.

Echoplex circuits suitable for use in block 42 are discussed in U.S. Patent No. 4,301,507 incorporated by reference herein. Serial I/O and parallel I/O port circuits are well known and will not be discussed further herein.

FIG. 10 and FIG. 11 are timing diagrams showing the interrelationship of signals previously discussed. The designated parameters and preferred timing are shown in TABLE III. It is believed that these diagrams will be readily understood by those skilled in the art so they will not be further described except with regard to the operation of the circuit.

TABLE III

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
t_{ALE}	ALE STROBE WIDTH	75		ns	CONDITION
t_{AHS}	A8-15 SET-UP TIME	50		ns	CONDITION
t_{ALS}	AD0-7 SET-UP TIME	40		ns	CONDITION
t_{ALH}	AD0-7 HOLD TIME	30		ns	CONDITION
t_{ARW}	ALE TO RD\ OR WR\ STROBE	125		ns	CONDITION
t_{RDW}	RD\ STROBE WIDTH	225		ns	CONDITION
t_{WRW}	WR\ STROBE WIDTH	220		ns	CONDITION
t_{WS}	WRITE DATA SET-UP TIME	50		ns	CONDITION
t_{INW}	INTERRUPT PULSE WIDTH	125		ns	
t_{ACC}	ALE TO VALID DATA		300	ns	
t_{ALD}	ALE TO VALID A8-7		50	ns	t_{ACCMAX} - 250ns
$t_{(CE)PD}$	A8-15 TO :				
	ROM\ ENABLE STROBE		50	ns	t_{ACCMAX} - 250ns + t_{AHMIN}
	RAM\ ENABLE STROBE		50	ns	t_{ACCMAX} - 250ns + t_{AHMIN}
	NVM1\ ENABLE STROBE		60	ns	t_{ACCMAX} - 280ns + t_{AHMIN}
	NVM2\ ENABLE STROBE		60	ns	t_{ACCMAX} - 280ns + t_{AHMIN}
	ECHO/VOID\ STROBE		70	ns	t_{ACCMAX} - 280ns + t_{AHMIN}
t_{DS}	INPUT PORT DATA SET-UP TIME	50		ns	
t_{WH}	WRITE DATA HOLD TIME	75		ns	
t_{NWD}	WR\ TO NVMWR\ DELAY		35	ns	t_{WHMIN} - t_{NWDMAX}
t_{NVMH}	WRITE DATA HOLD TIME AFTER NVMWR\		50	ns	t_{WHMIN} - t_{NWD}
t_{DO}	WR\ TO OUTPUT PORT DATA VALID		75	ns	t_{WHMIN}
t_{RH}	A8-7 HOLD TIME AFTER RD\	0		ns	
t_{RDH}	DATA HOLD TIME AFTER RD\	0	50	ns	
t_{RWI}	RD\ OR WR\ TO INTR\		90	ns	
t_{DMLT}	DMLDIS\ TO A8-7 FLOAT		25	ns	
t_{EXT}	EXTDEC\ to CE's FLOAT		25	ns	

The operation of the circuit has been particularly described with respect to each of the functional units. Broadly, however, the circuit 10 in accordance with the invention receives and decodes the periodic address signals communicated from the microprocessor and received at decoder block 28 and control flip-flop block 32. The address signals are decoded to provide an "active" selection signal for each of the various blocks of the circuit 10 and the memory devices of the electronic postage meter depending upon the communication of the appropriate addresses for the particular device. In the event that an illegal address is communicated either because of a microprocessor or software failure or because of a failure in the instant circuit, the $\overline{\text{DVOID}}$ signal from the decoder block 28 goes "active" causing the output of gate 106 (FIG. 6) to go high and latching the Q output of flip-flop 108 active. Thus a latched interrupt signal is sent to the interrupt control block 50 for communication to the microprocessor which responds as previously described above in conjunction with FIG. 9 whenever an illegal access is attempted.

As discussed previously, further protection is provided in the event that both nonvolatile memories are selected. As seen in FIG. 7, if both the $\overline{\text{NVM1}}$ and the $\overline{\text{NVM2}}$ signals are active the output of gate 128 is high. This output is inverted and applied to gate 124 whose output is then held high so long as both devices are selected. The output of 124 is inverted and the low input to gate 126 blocks the microprocessor's write strobe WR to the NVM. It

will also be appreciated that an additional interlock exists on the write access to each NVM by way of control flip-flops WR1-EN and WR2-EN. Under software control, write access is provided to NVM1 only when WR1-EN is set. Similarly, write access is provided to NVM2 only when WR2-EN is set.

Protection is also provided during system power up with the use of the unlock control flip-flop signal. It is a master control of access to the NVM's and postage printing which will disable these functions until the software operating system is ready to enable them.

In order to assure that signal $\overline{\text{NVMWR}}$, the output from gate 126 is not shorted active and so to assure that writing to the NVM is being commanded by the microprocessor, the selection of a nonvolatile memory is blocked if $\overline{\text{NVMWR}}$ is held active. The output write enable signal $\overline{\text{NVMWR}}$ is fed to latch 130 (FIG. 7) which is clocked by the address-latch-enable signal (ALE) from the microprocessor. The Q output from the latch which is normally high is used to enable gates 132 and 134.

If $\overline{\text{NVMWR}}$ is active when the ALE signal becomes active, the Q output of latch 130 goes high and blocks the output of gates 132 and 134. Thus in order for a nonvolatile memory to be selected there must be a periodically active nonvolatile memory write enabling signal and selection of only one nonvolatile memory to assure that the microprocessor is providing the appropriate data to the appropriately selected NVM.

It will be understood that the claims are intended to cover all changes and modifications of the embodiment herein chosen for the purpose of illustration which do not constitute departures from the scope and spirit of the invention.

What is claimed is:

1. In a postage meter having a microprocessor for controlling the printing of value and for accounting for the printing of such value and at least two nonvolatile memories for storing information, said microprocessor being operative to read information from and write information to said nonvolatile memories, said microprocessor providing a write strobe signal operative for enabling writing of information into said nonvolatile memories, nonvolatile memory selection means comprising a logic circuit for selecting one of said nonvolatile memories in accordance with information from the microprocessor, and means for blocking said write strobe signal to said nonvolatile memories when neither of said nonvolatile memories is selected.

2. The electronic postage meter of claim 1 including means for blocking the write strobe signal whenever both nonvolatile memories are simultaneously selected.

3. The electronic postage meter of claim 1 further comprising means for preventing the selection of either of said nonvolatile memories in the event that the write strobe signal communicated to said nonvolatile memories is held in an active state.

4. The electronic postage meter of claim 3 wherein said means for preventing includes latching means for continuously blocking the selection of either of said nonvolatile memories.

FIG. 1

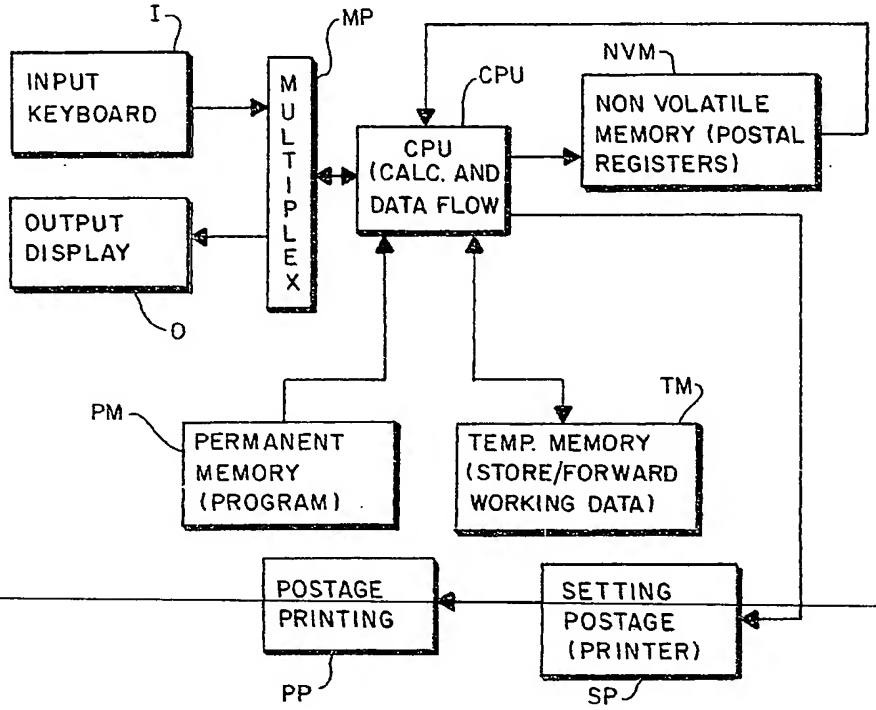
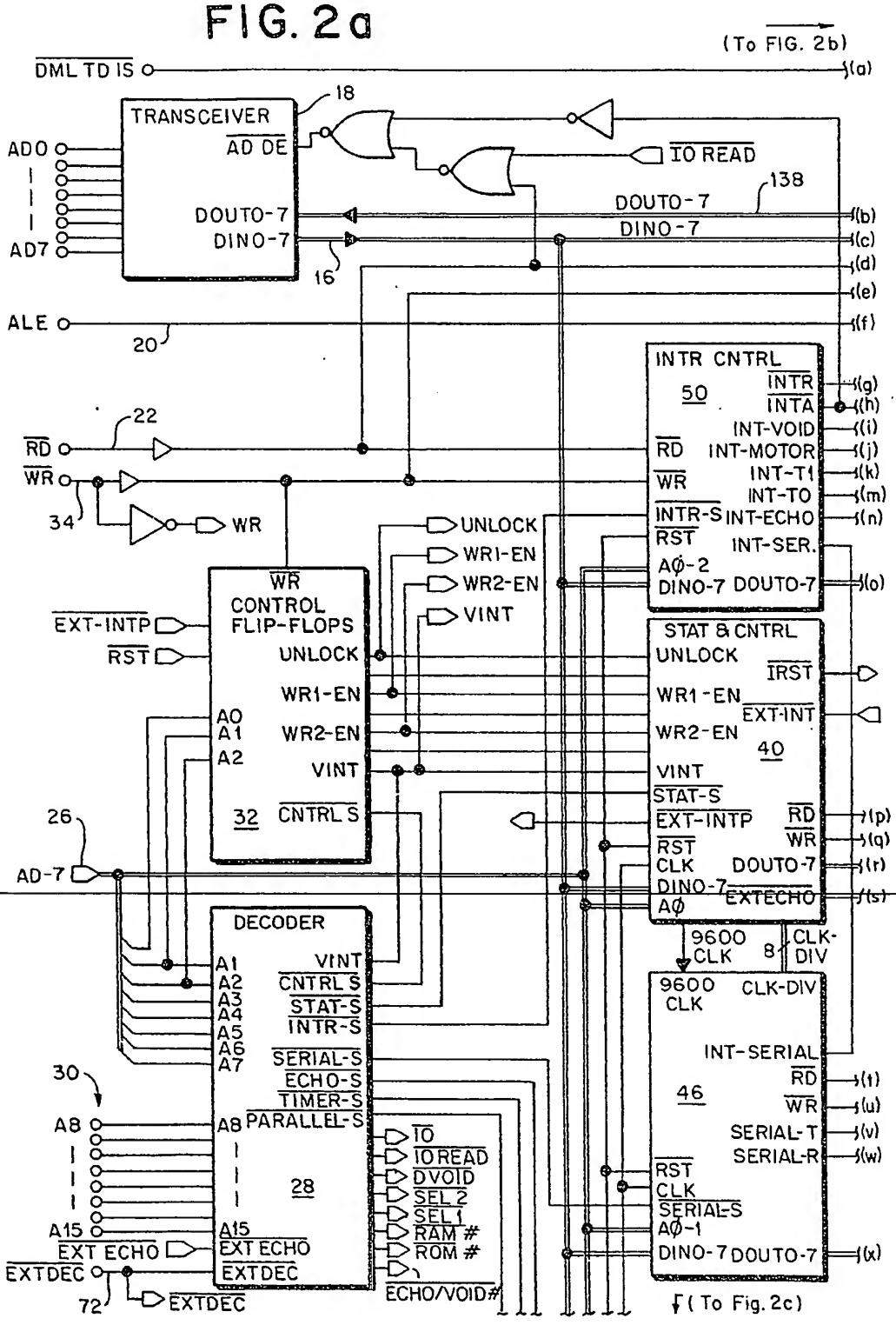

I
MP
INPUT KEYBOARD
MULTIPLEX
CPU
NVM
CPU (CALC. AND DATA FLOW
NON VOLATILE MEMORY (POSTAL REGISTERS)
OUTPUT DISPLAY
O
PM
TM
PERMANENT MEMORY (PROGRAM)
TEMP. MEMORY (STORE/FORWARD WORKING DATA)
POSTAGE PRINTING
SETTING POSTAGE (PRINTER)
PP
SP

FIG. 2a


(To FIG. 2b)
DML TD IS
(a)
TRANSCEIVER
18
AD DE
AD0
AD7
DOUTO-7
DINO-7
16
IO READ
138
DOUTO-7
DINO-7
(b)
(c)
(d)
(e)
(f)
ALE
20
INTR CNTRL
50
INTR
INTA
INT-VOID
RD
INT-MOTOR
WR
INT-T1
INT-TO
INTR-S
INT-ECHO
RST
INT-SER.
AØ-2
DINO-7
DOUTO-7
(g)
(h)
(i)
(j)
(k)
(m)
(n)
(o)
22
RD
WR
34
WR
UNLOCK
WR1-EN
WR2-EN
VINT
WR
CONTROL
FLIP-FLOPS
EXT-INTP
RST
UNLOCK
WR1-EN
A0
A1
WR2-EN
A2
VINT
32
CNTRL S
STAT & CNTRL
UNLOCK
IRST
WR1-EN
EXT-INT
WR2-EN
40
VINT
STAT-S
EXT-INTP
RD
WR
RST
CLK
DOUTO-7
DINO-7
EXTECHO
AØ
(p)
(q)
(r)
(s)
26
AD-7
DECODER
A1
A2
A3
A4
A5
A6
A7
A8
A15
EXT ECHO
EXTDEC
VINT
CNTRL S
STAT-S
INTR-S
SERIAL-S
ECHO-S
TIMER-S
PARALLEL-S
28
30
72
EXTDEC
IO
IO READ
DVOID
SEL 2
SEL 1
RAM #
ROM #
ECHO/VOID#
9600
CLK
8
CLK-
DIV
9600
CLK
CLK-DIV
INT-SERIAL
RD
WR
46
SERIAL-T
SERIAL-R
RST
CLK
SERIAL-S
AØ-1
DINO-7
DOUTO-7
(t)
(u)
(v)
(w)
(x)
(To Fig. 2c)

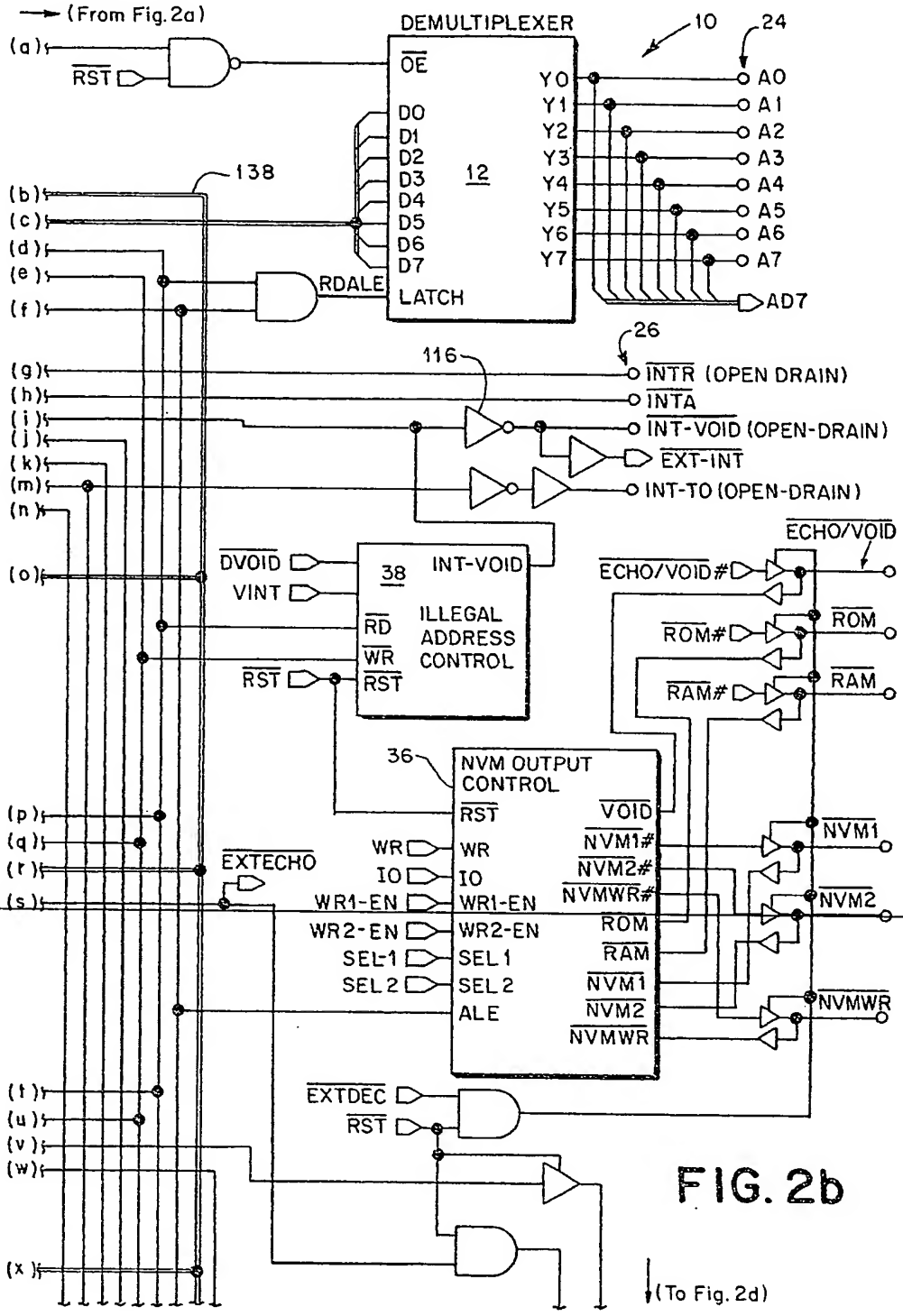
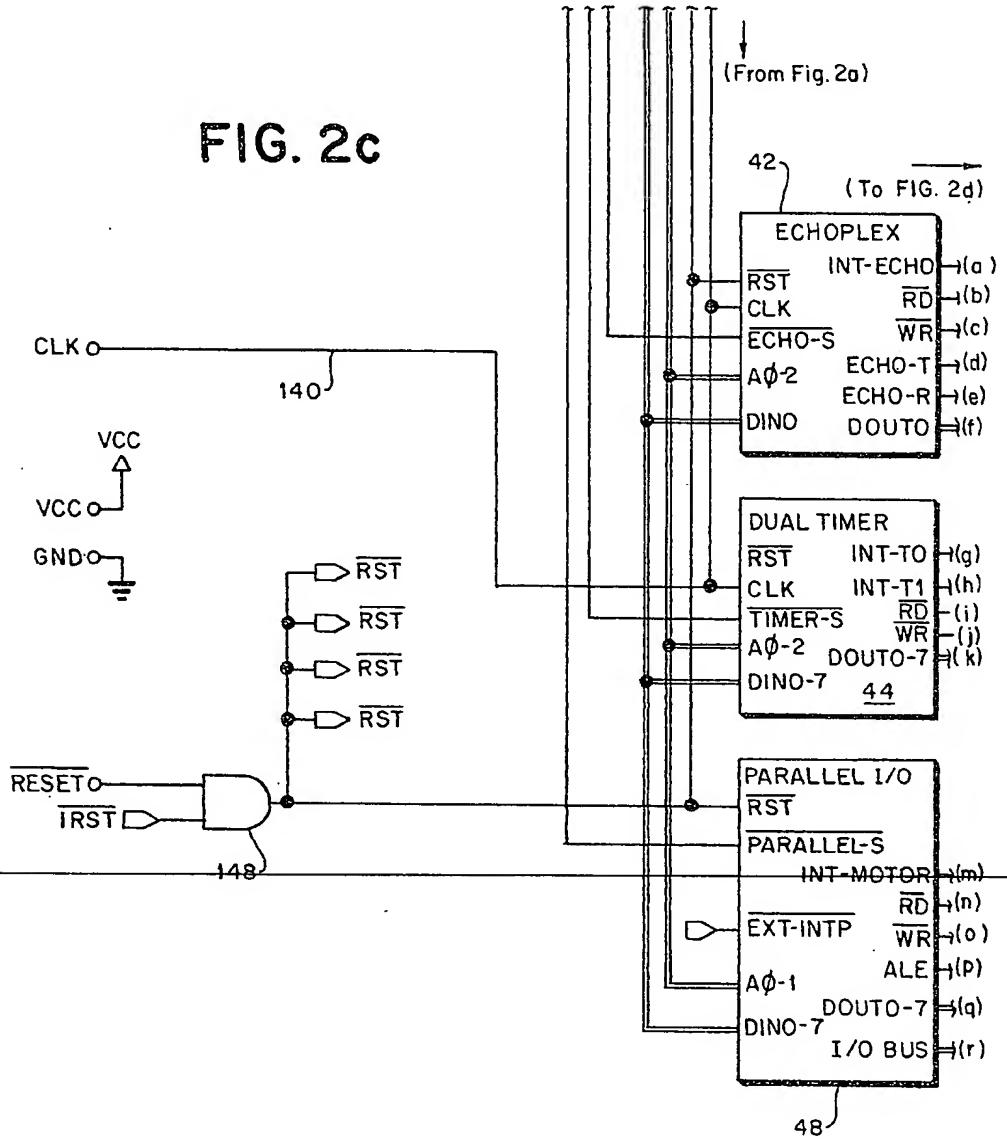

(From Fig. 2a)
DEMULTIPLEXER
10
24
OE
RST
D0
D1
D2
D3
D4
D5
D6
D7
12
LATCH
RDALE
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
A0
A1
A2
A3
A4
A5
A6
A7
AD7
138
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
(j)
(k)
(m)
(n)
(o)
(p)
(q)
(r)
(s)
(t)
(u)
(v)
(w)
(x)
26
116
INTR (OPEN DRAIN)
INTA
INT-VOID (OPEN-DRAIN)
EXT-INT
INT-TO (OPEN-DRAIN)
ECHO/VOID
DVOID
VINT
38
INT-VOID
ILLEGAL ADDRESS CONTROL
RD
WR
RST
ECHO/VOID#
ROM#
RAM#
ROM
RAM
36
NVM OUTPUT CONTROL
VOID
NVM1#
NVM2#
NVMWR#
ROM
RAM
NVM1
NVM2
NVMWR
EXTECHO
WR
IO
WR1-EN
WR2-EN
SEL1
SEL2
ALE
EXTDEC
(To Fig. 2d)

FIG. 2b

FIG. 2c


(From Fig. 2a)
42
(To FIG. 2d)
ECHOPLEX
RST
CLK
ECHO-S
AΦ-2
DINO
INT-ECHO
RD
WR
ECHO-T
ECHO-R
DOUTO
(a)
(b)
(c)
(d)
(e)
(f)
DUAL TIMER
RST
CLK
TIMER-S
AΦ-2
DINO-7
INT-T0
INT-T1
RD
WR
DOUTO-7
44
(g)
(h)
(i)
(j)
(k)
PARALLEL I/O
RST
PARALLEL-S
INT-MOTOR
RD
WR
EXT-INTP
AΦ-1
ALE
DOUTO-7
DINO-7
I/O BUS
(m)
(n)
(o)
(p)
(q)
(r)
48
CLK
140
VCC
VCC
GND
RST
RST
RST
RST
RESET
IRST
148

1247252

21-5

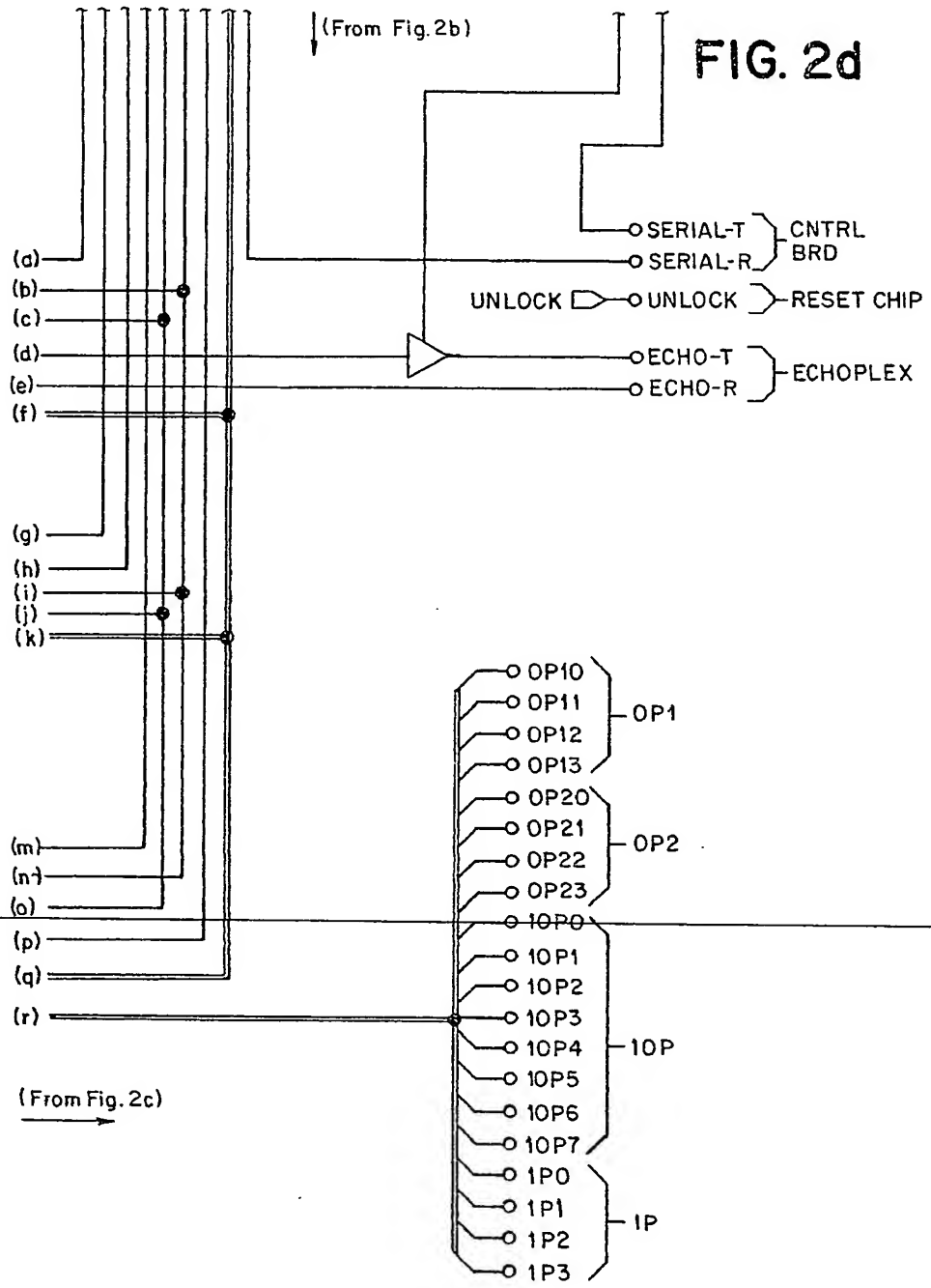
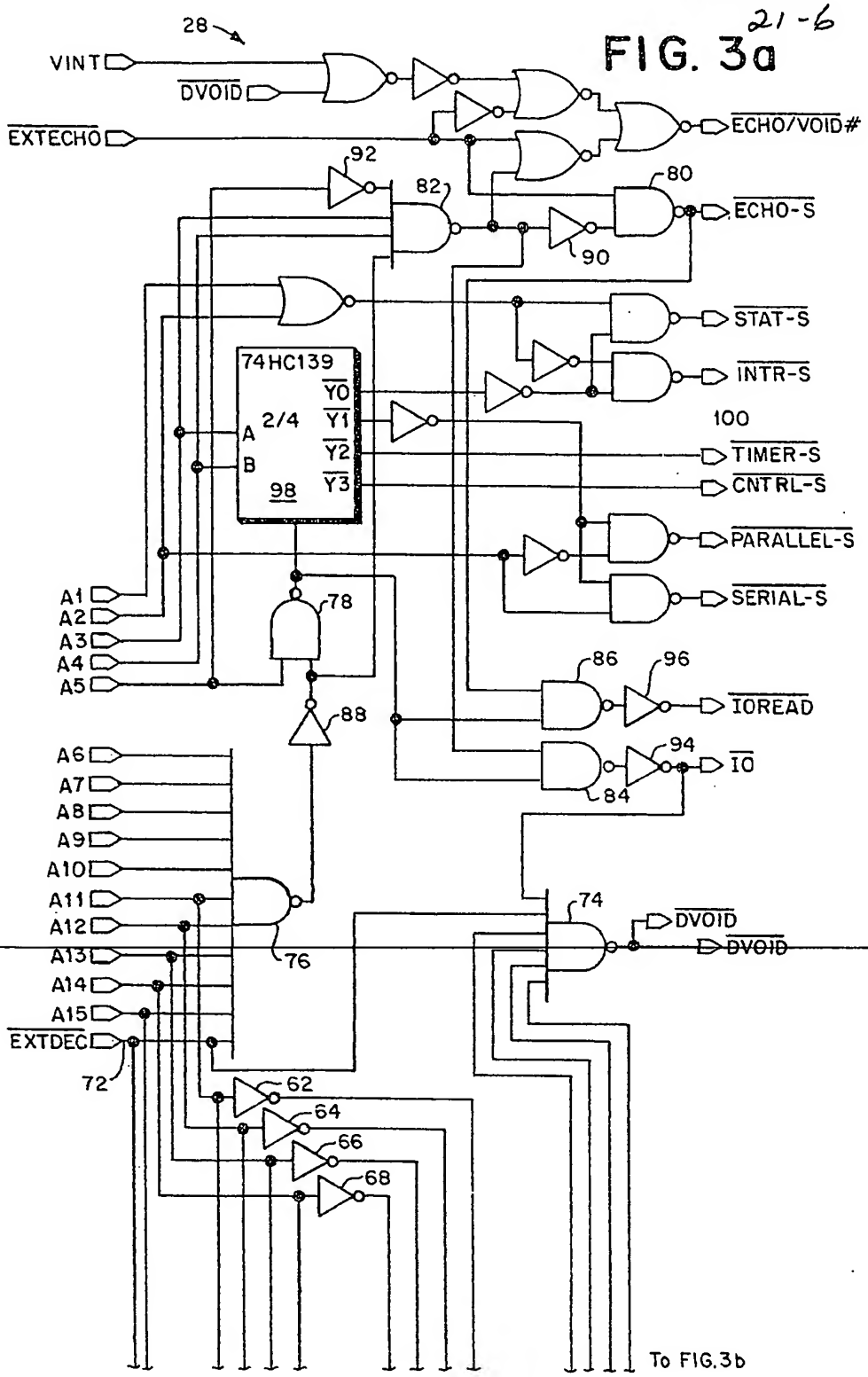
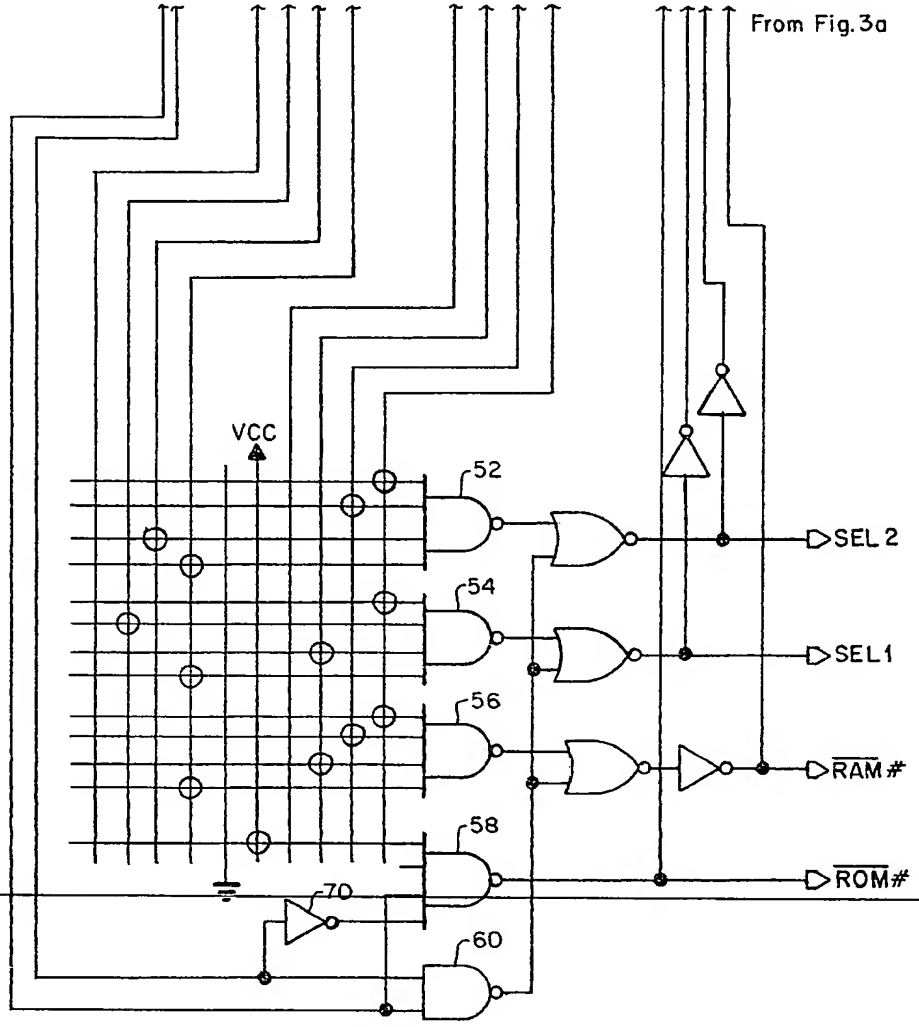


FIG. 2d

FIG. 3a


28
VINT
DVOID
EXTECHO
ECHO/VOID#
92
82
80
ECHO-S
90
STAT-S
INTR-S
74HC139
Y0
2/4
Y1
A
Y2
B
Y3
98
100
TIMER-S
CNTRL-S
PARALLEL-S
SERIAL-S
A1
A2
A3
A4
A5
78
86
96
IOREAD
88
94
IO
84
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
EXTDEC
72
76
74
DVOID
DVOID
62
64
66
68
To FIG.3b



⊕ INDICATES DEFAULT METALIZATION CONTACTS

FIG. 3b

Consumer and Corporate Affairs Canada
Consommation et Corporations Canada

(11) (A) No. 1 247 252

(45) ISSUED 881220

(52) CLASS 354-237
C.R. CL. 354-34

(51) INT. CL.[4] G07B 17/02

(19) (CA) **CANADIAN PATENT** (12)

(54) Electronic Postage Meter Having Non-Volatile Memory Selection Means

(72) DiGiulio, Peter C.;
Stalzer, Henry,
U.S.A.

(73) Granted to Pitney Bowes, Inc.
U.S.A.

(21) APPLICATION No. 503,779

(22) FILED 860311

(30) PRIORITY DATE U.S.A. (710,871) 850312

No. OF CLAIMS 4

Canada

DISTRIBUTED BY THE PATENT OFFICE, OTTAWA.
CCA-274 (11-82)

508777

ELECTRONIC POSTAGE METER HAVING NONVOLATILE MEMORY SELECTION MEANS

Abstract

An electronic postage meter having an improved memory selection circuit is disclosed. A custom memory map decoder circuit with resolution down to a single byte location is used to provide selection enabling signals to insure the selection of an appropriate device only when the addresses appropriate to that device are communicated. In accordance with the invention, at least two nonvolatile memories are provided. Writing to either of these nonvolatile memories is inhibited unless one and only one memory is selected. The circuit also prevents the selection of either of the nonvolatile memories in the event that the write strobe signal to the memories is held active.

ELECTRONIC POSTAGE METER HAVING A NONVOLATILE MEMORY SELECTION MEANS

The invention relates to postage meters and in particular to electronic postage meters having microcomputer control of printing and accounting functions.

Devices of this type are generally known, and are discussed for example in U.S. Patent No. 3,978,457. This patent discloses a system for a postage meter which includes a keyboard for the manual introduction of data corresponding to the postage to be printed in a Random Access Memory for real time operation. Data is stored in a nonvolatile memory upon power down and read into the Random Access Memory upon power up.

U.S. Patent No. 4,481,604 describes an electronic postage meter having a redundant memory system in which for each postal printing operation identical data is stored, respectively, in two separate but identical CMOS battery-backed nonvolatile memories.

In these known devices, there have been found to be times when essential data has not properly been stored in the nonvolatile memory of the meter. It has been found that one reason might be the improper selection of access to a particular device.

In known electronic postage meters, the microprocessor high order address bits or combination thereof are utilized in a standard decoder for selecting or enabling a particular

memory or peripheral device to be accessed in accordance with the microcomputer instructions. While this normally works well, in many cases of improper operation of the microcomputer or failure of one of the address lines of the bus, an improper bit may be decoded and the select logic gate which then enables the wrong device may cause wrong data to be read from memory or in the worst case cause data to be written into an unknown memory or peripheral with no indication of any malfunction. When this happens there is a strong possibility of service personnel's not being able to recover essential information from the nonvolatile memory in the postage meter when the postage meter fails.

In accordance with the invention, at least two nonvolatile memories are provided. In order to assure that data is written only to a selected nonvolatile memory, a logic circuit is provided which will decode the addresses called by the microprocessor to select one of these Nonvolatile Memories and which will enable a write strobe signal from the microprocessor to communicate with the NVM only when one and only one memory is selected. The logic circuit also includes means for preventing the selection of either of the nonvolatile memories in the event that the write-strobe signal is held active.

It is accordingly an object of an aspect of the invention to provide a write strobe signal to the nonvolatile memory only when the appropriate addresses are communicated from the microprocessor so as to particularly insure the reading and

writing of the appropriate data into the appropriate location.

It is an object of an aspect of the invention to provide in an electronic postage meter a means for assuring that the information in nonvolatile memory may be altered only upon further verification that such altering is intended.

It is an object of an aspect of the invention to prevent the writing of information to Nonvolatile Memory under circumstances where such writing would at all times be enabled due to a malfunction in the Electronic Postage Meter.

An aspect of the invention is as follows:

In a postage meter having a mircroprocessor for controlling the printing of value and for accounting for the printing of such value and at least two nonvolatile memories for storing information, said microprocessors being operative to read ~~information from and write information to said nonvolatile~~ memories, said microprocessor providing a write strobe signal operative for enabling writing of information into said nonvolatile memories, nonvolatile memory selection means comprising a logic circuit for selecting one of said nonvolatile memories in accordance with information from the microprocessor, and means for blocking said write strobe signal to said nonvolatile memories when neither of said nonvolatile memories is selected.

Other features and objects of the invention will become apparent in conjunction with the description of the drawing wherein:

FIG. 1 is a block diagram of an electronic postage meter in accordance with the invention;

FIG. 2 is a block diagram of a specific arrangement of a processor interface circuit in accordance with the invention;

FIG. 3 is a schematic of a decoder arrangement in accordance with the invention;

FIG. 4 is a default memory map showing a preferred arrangement of memory locations in accordance with the invention;

FIG. 5 is an embodiment of a circuit for providing a plurality of control output signals for NVM access;

FIG. 6 shows a preferred embodiment for providing a signal in response to an illegal address selection;

FIG. 7 shows in schematic form a preferred embodiment of a circuit for providing NVM selection;

FIG. 8 shows in schematic form a status and control circuit arrangement;

FIG. 9 is a schematic of a circuit for control of interrupts to the system microprocessor;

FIG. 10 is a timing diagram of the events; and FIG. 11 is a timing diagram.

Referring now to FIG. 1 which is a block diagram of a meter in which the invention may be incorporated. Such meters are known and are described for instance in U.S. Patent No. 3,978,457 to Check, et al and assigned to the assignee of the present invention. In this patent, the working memory under control of the CPU is a Random Access Memory from which data must be transferred to a nonvolatile memory upon loss or shutdown of power to the meter.

U.S. Patent No. 4,481,604 assigned to Roneo Alcatel discloses an electronic postage meter where the Random Access Memory and the nonvolatile storage memories are combined in battery backed CMOS RAMs which are used both for the real time operation and for long term storage of information in postal registers. EPC Application No. 0 085 385 published August 10, 1983, and assigned to the assignee of the present invention discloses an improved dual non-memory system. It will be appreciated by those skilled in the art that such a device may be combined with the electronic postage meter described in Check and is also suitable for the invention disclosed herein. The decoder arrangement disclosed herein is conveniently used to provide a method and apparatus for further protecting essential postal data in conjunction with the circuit described in Canadian Application Serial No. 503,785 filed on even date herewith entitled POSTAGE METER WITH A NONVOLATILE MEMORY PROTECTION CIRCUIT and assigned to the assignee of the present invention.

Still referring to FIG. 1, the heart of the general functional arrangement of the system is the CPU which is utilized with specific instructions programmed in the Read Only Memory (PM), for the performance of control of the basic meter functions, for the performance of calculations based on any input data and for controlling the flow of data into the various memories.

The system, may operate in accordance with data applied from an appropriate input means "I" or from a communications means "C" such as described for instance in U.S. Patent No. 4,301,507 to Soderberg. The data is fed into the CPU under control of the program in Read Only Memory and at any time during the operation of the system, should the contents of the memory storing the appropriate credit/debit balances or other cumulations in accordance with various features of the system be desired to be displayed, appropriate instructions provided by the input means "I" cause the CPU to access the desired locations in memory which store the information requested.

The information may be displayed on an output unit "O". As well known, the input and output units may be multiplexed by a suitable multiplex unit "MP" for transferring data to and from the CPU.

FIG. 2 is a block diagram of a specific arrangement of a processor interface circuit in accordance with the invention and comprises an address decoder and associated selection circuitry for the selection and control of various elements of the Electronic Postage Meter. It will be appreciated that the circuit arrangement herein described is preferably embodied in a custom LSI microchip, however, it will be understood that the use of conventional logic components is also contemplated.

Turning now to FIG. 2, the overall block diagram of the circuit is shown generally at 10. The demultiplexer 12 in conventional manner demultiplexes the address/data bus 14 of a microprocessor (not shown in FIG. 2), suitably an 8085 series microprocessor available from the Intel Corporation or an NSC800 series microprocessor available from the National Semiconductor Corporation. The bus 14 communicates with the demultiplexer 12 on communication lines 16 through a conventional transceiver circuit arrangement 18. For best results the ADDRESS LATCH ENABLE (ALE) signal 20 from the microprocessor is "anded" with the microprocessor read strobe signal 22 to provide the latching signal for latching the address information for the demultiplexer 12.

The demultiplexed address information is fed out on lines 24 for use in other parts of the EPM and are internally

connected at 26 to the decoder section 28. The high order address signals directly from the microprocessor are communicated on lines 30 to the decoder section 26. An external decode signal, $\overline{\text{EXTDEC}}$, is also input to the decoder section 28.

The decoder section 28 receives and decodes a complete input address received at 26 and 30 to provide select outputs for the various parts of the system. The low order demultiplexed address lines AØ, Al and A2 are utilized as inputs to control flip-flops 32 along with the microprocessor write strobe $\overline{\text{WR}}$ received at 34 from the microprocessor. As described further below, the control flip-flop section generates four control signals in response to these inputs in addition to a decoder reset signal and other derived signals, i.e. EXT-INTP, a pulse signal generated at the activation of the illegal memory access output pin, and a select signal CONTRL-s for the selection of the Control Flip Flop block.

Outputs from the decoder 28 are provided to NVM output control block 36. This control block 36 in accordance with the invention provides a fail-safe NVM device selection. The selection of either NVM is disabled if the NVM write line is shorted to the "active" state. The NVM write strobe is disabled whenever the other devices are selected or in the event that both NVMs are simultaneously selected.

In accordance with the invention, an illegal address control block 38, in conjunction with the decoder 28 detects when the microprocessor read or write strobes attempt to access addresses an illegal, i.e. unused, memory space and,

as discussed below, provides a signal output for interrupting the processor.

Status and control block 40 monitors the outputs from the control Flip-Flop section and provides a control port to generate a decoder reset and to control the selection of an internal or external communication through an "Echoplex" I/O section 42. Preferably the section also includes an 8-bit timer to set the Transmit Baud rate for the serial communications.

Dual Timer section 44 provides two programmable 16-bit timers. Preferably the system clock is the clock input to the timers. Suitably each is programmable for continuous or for one-shot operation for generating an interrupt when the programmed count is completed. Conveniently an 8-bit counter divider can be selected to prescale the clock input or the ripple output of the first timer may be selected as the clock input to the second timer.

Conveniently serial I/O block 46 and parallel I/O block 48 are utilized for communication with a keyboard and display and for motor control, sensing postal value and miscellaneous control functions.

For best results, an Interrupt Status and Control Block 50 is provided along with an interrupt mask control port for enabling selected interrupts to interrupt the systems processor.

FIG. 3 shows a schematic of an embodiment of a decoder block for providing a decoded memory map in accordance with the invention. The crossed lines with a circle superposed

are used to indicate the preferred conductive path in a customized chip arrangement. It will be appreciated that the illustrated arrangement is extremely convenient in that the decoded memory map as described below may be modified easily with only a few mask changes.

The various addresses communicated in known manner from the microprocessor and demultiplexer as described previously are each fed to leads A1 through A15 of the decoder block 28. The address bits on address lines A11 through A15 are supplied to NAND gates 52, 54, 56, 58, and 60 and inverted at inverters 62, 64, 66, 68, and 70 and applied as illustrated to the NAND gates 52, 54, 56, and 58. An external decode signal 72 (see also FIG. 2) is applied to NAND gate 60. The output of NAND gate 60 is NOR'D with the outputs of gates 52, 54, and 56. The EXTDEC signal is also applied directed to gate 58. It will be noted that when "active" this signal will disable the decode function. The decoded outputs from the connections illustrated in FIG. 3 for the preferred embodiment are as shown in Table I and in FIG. 4.

TABLE I

OUTPUTS

ROM#	: SELECT FOR EXTERNAL PROM MEMORY
RAM#	: SELECT FOR EXTERNAL RAM MEMORY
SEL1	: FOR GENERATING THE SELECT FOR EXTERNAL NVM#1
SEL2	: FOR GENERATING THE SELECT FOR EXTERNAL NVM#2
CNTRL-S\	: SELECT FOR INTERNAL CONTROL FLIP-FLOP BLOCK
INTR-S\	: SELECT FOR INTERNAL INTERRUPT CONTROLLER
STAT-S\	: SELECT FOR INTERNAL STATUS BLOCK
TIMER-S\	: SELECT FOR INTERNAL DUAL-TIMER BLOCK
ECHO-S\	: SELECT FOR INTERNAL ECHOPLEX BLOCK
SERIAL-S\	: SELECT FOR INTERNAL SERIAL I/O BLOCK
PARALLEL-S\	: SELECT FOR INTERNAL PARALLEL I/O BLOCK
ECHO/VOID#\	: SELECT FOR EXTERNAL ECHOPLEX BLOCK OR SPARE DECODE SIGNAL WHEN UNUSED MEMORY SPACE IS SELECTED (OR NEITHER)
IO\	: ACTIVE WHEN ANY I/O SELECTS ARE ACTIVE
IOREAD\	: ACTIVE WHEN ANY OF THE INTERNAL SELECTS ARE ACTIVE
DVOID	: ACTIVE WHEN "ExtDec\" IS INACTIVE AND WHEN NONE OF THE SELECT OUTPUTS ARE ACTIVE

OUTPUT SIGNAL	ADDRESS RANGE(S)	SIZE
ROM#	ØØØØ - 7FFF	32 KBYTES
RAM#	CØØØ - C7FF	2 KBYTES
SEL1	DØØØ - D7FF	2 KBYTES
SEL2	EØØØ - E7FF	2 KBYTES
ECHO-S\	FFD8 - FFDF	8 BYTES
STAT-S\	FFEØ - FFE1	2 BYTES
INTR-S\	FFE2 - FFE7	6 BYTES
PARALLEL-S\	FFE8 - FFEB	4 BYTES
SERIAL-S\	FFEC - FFEF	4 BYTES
TIMER-S\	FFFØ - FFF7	8 BYTES
CNTRL-S\	FFF8 - FFFF	8 BYTES
IO\	FFD8 - FFFF	48 BYTES
IOREAD\	FFD8 - FFFF; IF "EXTECHO\" INACTIVE FFEØ - FFFF; IF "EXTECHO\" ACTIVE	

It will be noted that in accordance with the invention, an active DVOID output is provided from NAND gate 74 when none of the system's blocks are selected. It will also be clear to one skilled in the art that the address bits, when appropriately decoded as in the illustrated circuit by NAND gates 76, 78, 80, 82, 84, and 86 and inverters 88, 90,

92, 94, and 96 provide an "active" output IO whenever any of the I/O functions is selected and an "active" I/O read output whenever any of the internal circuit functional blocks are selected. Address bits A3 and A4 are applied to 2-to-4 demultiplexer 98 and decoded with other low order address bits for providing output signals as defined in Table I for selecting the appropriate blocks.

It will be understood that the signal DVOID is not necessarily limited to its previously described function. For instance, in the illustrated embodiment, a signal VINT from the control flip-flop block further described below may be used to convert this DVOID signal to another decode output. This signal shown as "ECHO/VOID" in FIG. 3 is available if the circuits internal ECHOPLEX block 42 is utilized. Alternatively it will be seen that if an external "echoplex" section is utilized, that is, when the signal "EXTECHO" is "active" the "ECHO/VOID#" output becomes the "select" signal for the external block and the "select" signal for the internal echoplex section, "ECHO-S" is disabled.

As mentioned previously, the Control Flip-Flop section 32, more particularly shown in FIG. 5, generates four control output signals and their complements for controlling the generation of an illegal address interrupt signal to the processor, to provide an independent enable/disable for the access to two separate NVM storage devices, to enable and disable meter postage printing and access to nonvolatile storage.

As best seen in FIG. 5 the low order address signals A0, A1, and A2 are fed to a 3-to-8 Line Decoder Multiplexer 102 equivalent to a 74HC138 available from RCA to set and reset flip-flops 104, 106, 108, and 110. The processor strobe signal $\overline{WR}$ and the select signal $\overline{CNTRL-S}$ are applied to the enable inputs of decoder 102. As illustrated, it is apparent that the control flip-flops are selectively controlled when both these signals are "active".

The decoder reset signal $\overline{RST}$ and $\overline{EXT-INTP}$ (a pulse signal generated at the activation of the illegal memory access interrupt signal) are "NAND'D" at "NAND" gate 112, inverted at inverter and applied to each of the flip-flops 104 and 110. Table II shows the preferred decoded control signals in response to the appropriate addresses.

TABLE II

AØ-2	DECODED CNTRL	FLIP-FLOP	OUTPUT	
Ø	VINT-CLR\	VINT	INACTIVE	
1	VINT-EN\	VINT	ACTIVE	PRESET
2	WR2-RESET\	WR2-EN	INACTIVE	PRESET
3	WR2-SET\	WR2-EN	ACTIVE	
4	WR1-RESET\	WR1-EN	INACTIVE	PRESET
5	WR1-SET\	WR1-EN	ACTIVE	
6	UNLOCK-SET\	UNLOCK	ACTIVE	
7	UNLOCK-CLR\	UNLOCK	INACTIVE	PRESET

The outputs from flip-flop 104 designated UNLOCK are preferably active to enable postage printing and for NVM access. For best results, the preset value is inactive to prevent printing and NVM access. The signal WR1-EN and WR2-EN are "active" for write access to respective NVM devices #1

and #2. Again, for best results the preset values are "inactive".

The output VINT which as previously discussed is fed to the decoder section 28 is active to enable an interrupt generation whenever an illegal memory access is attempted. It will be appreciated that this is preferred since in the "inactive" state it may be used to reset the generated interrupt signal or to disable the interrupt so that it may be used as a spare decode output. The VINT preset signal is "active" to enable the interrupt.

The illegal address control block 38 is shown more particularly in FIG. 6. This circuit is used to provide an indication of when access to unused memory space is attempted.

The $\overline{\text{DVOID}}$ decoded signal output from the decoder section 28 is nanded at NAND gate 106 with the $\overline{Q}$ output from a D Flip-Flop 108. The processors read strobe $\overline{RD}$ and write strobe $\overline{WR}$ are NAND'D at NAND gate 110, inverted and applied to the clock input of the D flip-flop 108. The decoder reset signal is NANDED with the "VINT" signal from the control flip-flop section 32 at NAND gate 112 and applied to the RESET input shown as $\overline{CLR}$ in the Figure.

Thus, depending upon the status of the signal VINT as discussed previously, the decoded void memory space indication will be latched at the lead edge of either the read or the write strobe of the microprocessor to provide the output INT-VOID from the Q terminal of flip-flop 108. In accordance with the invention, the INT-VOID signal is

provided to the system microprocessor as an interrupt signal. Preferably this indication will remain latched until reset by the reset signal from the microprocessor.

Conveniently as seen in FIG. 2 the output is inverted at inverter 116 and supplied at 118 at $\overline{\text{INT-VOID}}$.

For best results, this $\overline{\text{INT-VOID}}$ output pin in open-drain so as to permit any of a number of open-drain outputs wire-ored to this pin to activate the output signal. This output pin is then suitably tapped as the input signal $\overline{\text{EXT-INT}}$ which is furnished to the Status and Control Block. There, this signal is provided as a status port bit and upon its actuation, a 1 clock period pulse is generated on signal $\overline{\text{EXT-INTP}}$. This $\overline{\text{EXT-INTP}}$ is provided from the status and control section to reset the control flip-flop and parallel I/O sections to their default (safe) states when the $\overline{\text{INT-VOID}}$ output pin is activated.

Turning now the FIG. 7, the NVM Output Control Block 36 is shown in greater detail. In order to insure secure accounting in the NVM the WRITE access to the two independent NVM devices is independently enabled and disabled under software control.

The NVM OUTPUT CONTROL will block the microprocessor write strobe WR unless either of the NVM decoded select signals SEL1 and SEL2 is available and the appropriate write enable signal from the control flip-flops are available at NAND gates 118 and 120. The output of these gates are inputs to NAND gate 122 whose output is applied to NAND gate 124.

The output of this gate is inverted and supplied to NAND gate 126.

The other signals applied to NAND gate 124 are the decoded select signals NVM1, NVM2, ROM, RAM and VOID are taken from the output drivers and applied to NAND gate 124, with NVM 1 and NVM2 being NOR'D at NOR gate 128 and inverted before being applied to 124. It will be appreciated that the write strobe WR is blocked if the appropriate memory space is not selected. It will also be appreciated that if both NVMs are selected simultaneously the write strobe will also be blocked.

A further protection feature is provided in the event that the NVM write strobe output is shorted "active". The address enable strobe at 20 is applied as the clock signal to a D flip-flop 130. If the $\overline{\text{NVMWR}}$ is shorted active, the ALE signal clocks the Q output low to block both of the NVM device selection signals at NAND gates 132 and 134.

FIG. 8 is a schematic of the status and control block. The block comprises a status port to allow monitoring of the control flip-flop outputs. The outputs of the control flip-flop block 32 are applied to buffer 136 for output to data bus 138, see also FIG. 2. The system clock input from 140 (see FIG. 2) is used in conventional fashion for timing the internal reset output by counting through D flip-flops 142, 144, and 146 to provide signal IRST which is the control signal for resetting all of the flip-flops in the circuit and is applied along with the System Reset to AND gate 148, (see FIG. 2).

The block select signal $\overline{\text{STAT-S}}$ for this block, the write strobe, read strobe, and lowest order address bit are decoded to clock the writing of data at octal flip-flop 150, for initiating a general decoder reset under the control of appropriate software commands and for setting a baud-rate divider circuit if desired. The $\overline{\text{EXTECHO}}$ signal from D flip-flop 152 is used as previously discussed for selection of an external communication device (not shown).

The Interrupt Controller block 50 is shown in more detail in FIG. 9. The interrupt controller in accordance with the invention provides great flexibility in the servicing of the various interrupt signals to the microprocessor. The signal INT-VOID from the illegal address control block 38, signals INT-TO and INT-TI generated by the time-out of timers in timer block 44, signal INT-ECHO from the ECHOPLEX block 42 which is "active" to indicate the start of an echoplex message, signal INT-SERIAL from serial I/O block 46 which is "active" when new data is received or when the port is read for sending data, and signal INT-MOTOR from PARALLEL I/O block 48 which is preferably "active" when an illegal motor control output has been communicated are each input to the INTERRUPT CONTROLLER block 50. The status of each of these signals may be read out directly from buffer 154 when the $\overline{\text{RD-INTR}}$ signal is "active".

Signal $\overline{\text{INTA}}$ from the system microprocessor is an interrupt acknowledge. It will be appreciated that if the INTA line is held or tied in the "inactive" state, each interrupt signal input applied through gates indicated

generally at 156 and fed to NAND gate 158 will create an interrupt request signal $\overline{\text{INTR}}$ for communication to the system's microprocessor. Preferably, mask bits may be fed as data on data input bus 16 for providing masking bits to D-flip-flops 160 for latching. The latched outputs from 160 are applied to gates 156 so that the interrupt request will be generated whenever an unmasked device requests service. The particular device requesting service may be determined by reading the status buffer 154. The interrupt lines are also coded at the gates indicated generally at 162 for feeding to latch 164 which also provides similar information.

Preferably, as shown, there is also included a vectored interrupt for the handling of service requests. As discussed previously, a non-masked interrupt results in the generation of an interrupt-request signal to the systems microprocessor. For best results, the microprocessor upon receiving this signal will transmit an interrupt acknowledge signal $\overline{\text{INTA}}$. This signal places the contents of the opcode latch 166 onto the data bus. In accordance with the invention, the processor interprets this data as an opcode, normally a call instruction for the microprocessor. Upon execution of the instruction, the microprocessor generates another $\overline{\text{INTA}}$ pulse to enable the lower vector latch 168. The encoding of bits on this latch as described above. The vector thus generated, desirably reflects a predetermined code representing the highest priority interrupt. The next $\overline{\text{INTA}}$ pulse, in response to the call of this OPCODE, will

place the data residing in latch 170, preferably the upper vector address data, onto the data bus 138.

The $\overline{\text{INTR-S}}$ signal is utilized to select this block. The low order address signals AØ through A2 are used as illustrated to decode the various control signals on the gates indicated generally at 140.

Echoplex circuits suitable for use in block 42 are discussed in U.S. Patent No. 4,301,507 incorporated by reference herein. Serial I/O and parallel I/O port circuits are well known and will not be discussed further herein.

FIG. 10 and FIG. 11 are timing diagrams showing the interrelationship of signals previously discussed. The designated parameters and preferred timing are shown in TABLE III. It is believed that these diagrams will be readily understood by those skilled in the art so they will not be further described except with regard to the operation of the circuit.

TABLE III

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
t_{ALE}	ALE STROBE WIDTH	75		ns	CONDITION
t_{AHS}	A8-15 SET-UP TIME	50		ns	CONDITION
t_{ALS}	AD0-7 SET-UP TIME	40		ns	CONDITION
t_{ALH}	AD0-7 HOLD TIME	30		ns	CONDITION
t_{ARW}	ALE TO RD\ OR WR\ STROBE	125		ns	CONDITION
t_{RDW}	RD\ STROBE WIDTH	225		ns	CONDITION
t_{WRW}	WR\ STROBE WIDTH	220		ns	CONDITION
t_{WS}	WRITE DATA SET-UP TIME	50		ns	CONDITION
t_{INW}	INTERRUPT PULSE WIDTH	125		ns	
t_{ACC}	ALE TO VALID DATA		300	ns	
t_{ALD}	ALE TO VALID A0-7		50	ns	t_{ACCMAX} - 250ns
$t_{(CE)PD}$	A8-15 TO :				
	ROM\ ENABLE STROBE		50	ns	t_{ACCMAX} - 250ns + t_{AHMIN}
	RAM\ ENABLE STROBE		50	ns	t_{ACCMAX} - 250ns + t_{AHMIN}
	NVM1\ ENABLE STROBE		60	ns	t_{ACCMAX} - 280ns + t_{AHMIN}
	NVM2\ ENABLE STROBE		60	ns	t_{ACCMAX} - 280ns + t_{AHMIN}
	ECHO/VOID\ STROBE		70	ns	t_{ACCMAX} - 280ns + t_{AHMIN}
t_{DS}	INPUT PORT DATA SET-UP TIME	50		ns	
t_{WH}	WRITE DATA HOLD TIME	75		ns	
t_{NWD}	WR\ TO NVMWR\ DELAY		35	ns	t_{WHMIN} - t_{NWDMAX}
t_{NVMH}	WRITE DATA HOLD TIME AFTER NVMWR\		50	ns	t_{WHMIN} - t_{NWD}
t_{DO}	WR\ TO OUTPUT PORT DATA VALID		75	ns	t_{WHMIN}
t_{RH}	A0-7 HOLD TIME AFTER RD\	0		ns	
t_{RDH}	DATA HOLD TIME AFTER RD\	0	50	ns	
t_{RWI}	RD\ OR WR\ TO INTR\		90	ns	
t_{DMLT}	DMLDIS\ TO A0-7 FLOAT		25	ns	
t_{EXT}	EXTDEC\ to CE's FLOAT		25	ns	

The operation of the circuit has been particularly described with respect to each of the functional units. Broadly, however, the circuit 10 in accordance with the invention receives and decodes the periodic address signals communicated from the microprocessor and received at decoder block 28 and control flip-flop block 32. The address signals are decoded to provide an "active" selection signal for each of the various blocks of the circuit 10 and the memory devices of the electronic postage meter depending upon the communication of the appropriate addresses for the particular device. In the event that an illegal address is communicated either because of a microprocessor or software failure or because of a failure in the instant circuit, the $\overline{\text{DVOID}}$ signal from the decoder block 28 goes "active" causing the output of gate 106 (FIG. 6) to go high and latching the Q output of flip-flop 108 active. Thus a latched interrupt signal is sent to the interrupt control block 50 for communication to the microprocessor which responds as previously described above in conjunction with FIG. 9 whenever an illegal access is attempted.

As discussed previously, further protection is provided in the event that both nonvolatile memories are selected. As seen in FIG. 7, if both the $\overline{\text{NVM1}}$ and the $\overline{\text{NVM2}}$ signals are active the output of gate 128 is high. This output is inverted and applied to gate 124 whose output is then held high so long as both devices are selected. The output of 124 is inverted and the low input to gate 126 blocks the microprocessor's write strobe WR to the NVM. It

will also be appreciated that an additional interlock exists on the write access to each NVM by way of control flip-flops WR1-EN and WR2-EN. Under software control, write access is provided to NVM1 only when WR1-EN is set. Similarly, write access is provided to NVM2 only when WR2-EN is set.

Protection is also provided during system power up with the use of the unlock control flip-flop signal. It is a master control of access to the NVM's and postage printing which will disable these functions until the software operating system is ready to enable them.

In order to assure that signal $\overline{\text{NVMWR}}$, the output from gate 126 is not shorted active and so to assure that writing to the NVM is being commanded by the microprocessor, the selection of a nonvolatile memory is blocked if $\overline{\text{NVMWR}}$ is held active. The output write enable signal $\overline{\text{NVMWR}}$ is fed to latch 130 (FIG. 7) which is clocked by the address-latch-enable signal (ALE) from the microprocessor. The Q output from the latch which is normally high is used to enable gates 132 and 134.

If $\overline{\text{NVMWR}}$ is active when the ALE signal becomes active, the Q output of latch 130 goes high and blocks the output of gates 132 and 134. Thus in order for a nonvolatile memory to be selected there must be a periodically active nonvolatile memory write enabling signal and selection of only one nonvolatile memory to assure that the microprocessor is providing the appropriate data to the appropriately selected NVM.

It will be understood that the claims are intended to cover all changes and modifications of the embodiment herein chosen for the purpose of illustration which do not constitute departures from the scope and spirit of the invention.

What is claimed is:

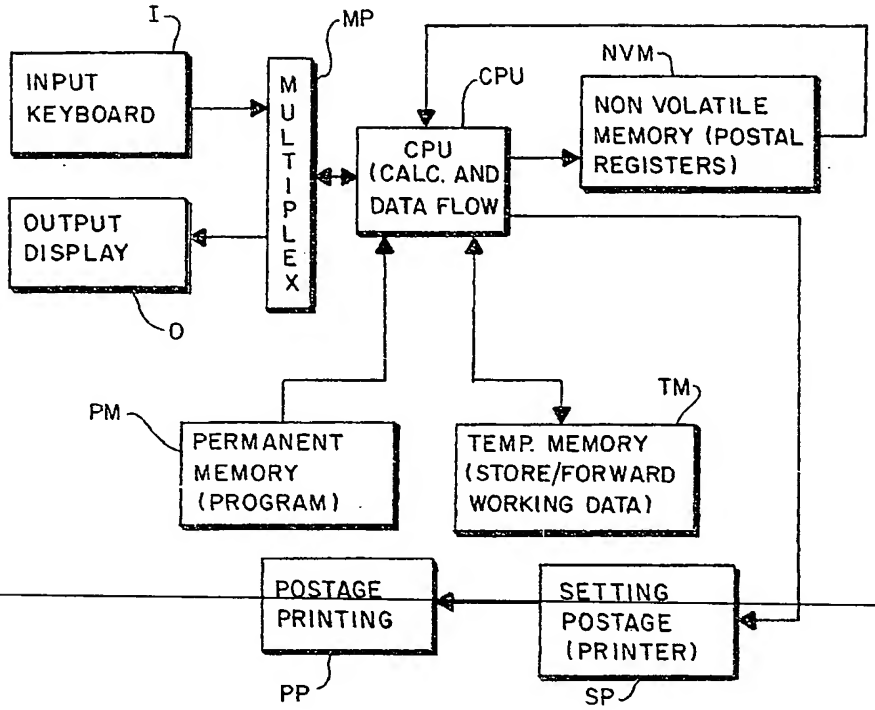
1. In a postage meter having a microprocessor for controlling the printing of value and for accounting for the printing of such value and at least two nonvolatile memories for storing information, said microprocessor being operative to read information from and write information to said nonvolatile memories, said microprocessor providing a write strobe signal operative for enabling writing of information into said nonvolatile memories, nonvolatile memory selection means comprising a logic circuit for selecting one of said nonvolatile memories in accordance with information from the microprocessor, and means for blocking said write strobe signal to said nonvolatile memories when neither of said nonvolatile memories is selected.

2. The electronic postage meter of claim 1 including means for blocking the write strobe signal whenever both nonvolatile memories are simultaneously selected.

3. The electronic postage meter of claim 1 further comprising means for preventing the selection of either of said nonvolatile memories in the event that the write strobe signal communicated to said nonvolatile memories is held in an active state.

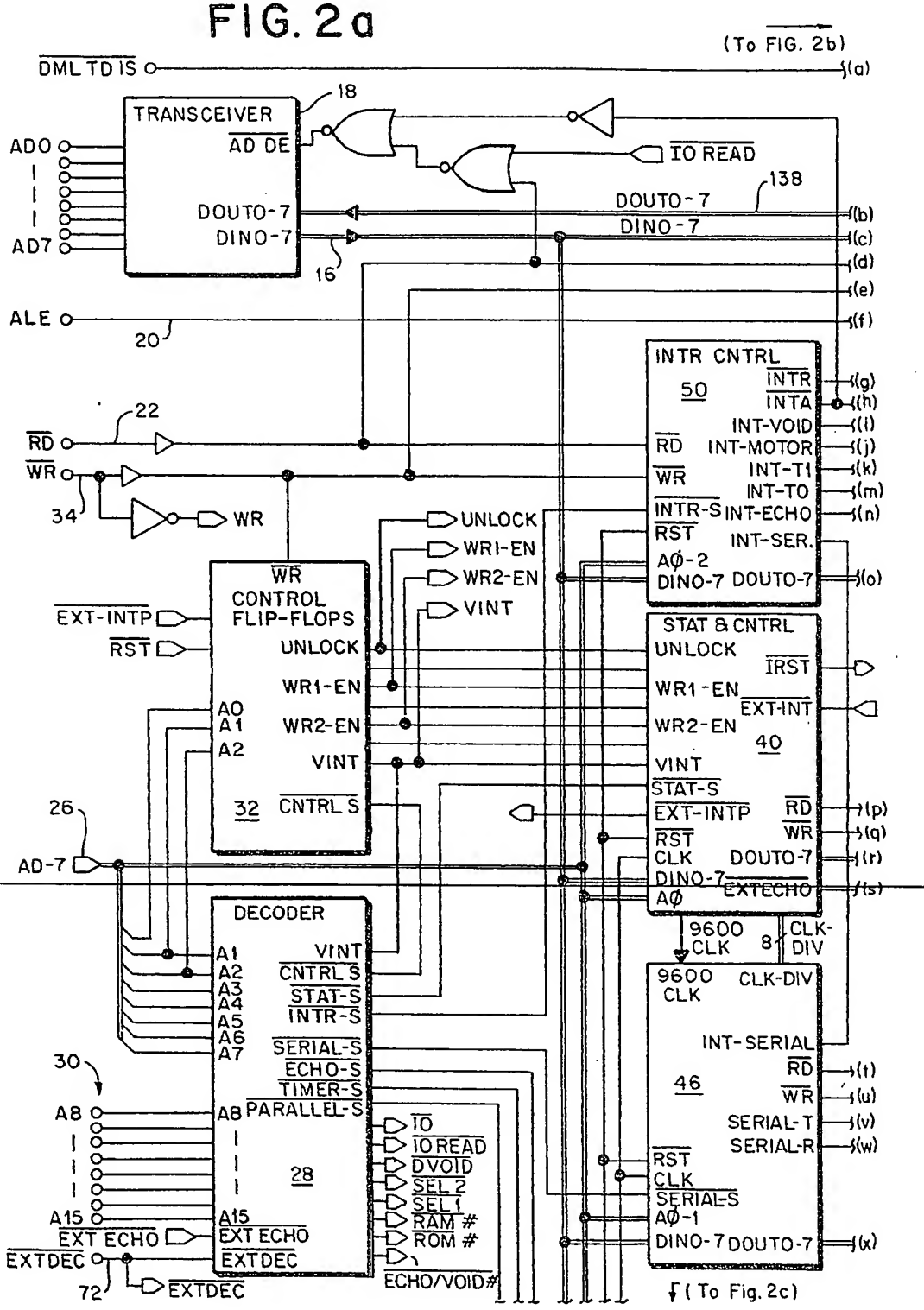
4. The electronic postage meter of claim 3 wherein said means for preventing includes latching means for continuously blocking the selection of either of said nonvolatile memories.

FIG. 1


I
MP
INPUT KEYBOARD
MULTIPLEX
NVM
CPU
NON VOLATILE MEMORY (POSTAL REGISTERS)
CPU (CALC. AND DATA FLOW
OUTPUT DISPLAY
O
PM
PERMANENT MEMORY (PROGRAM)
TM
TEMP. MEMORY (STORE/FORWARD WORKING DATA)
POSTAGE PRINTING
PP
SETTING POSTAGE (PRINTER)
SP

1247252
21-2

FIG. 2a



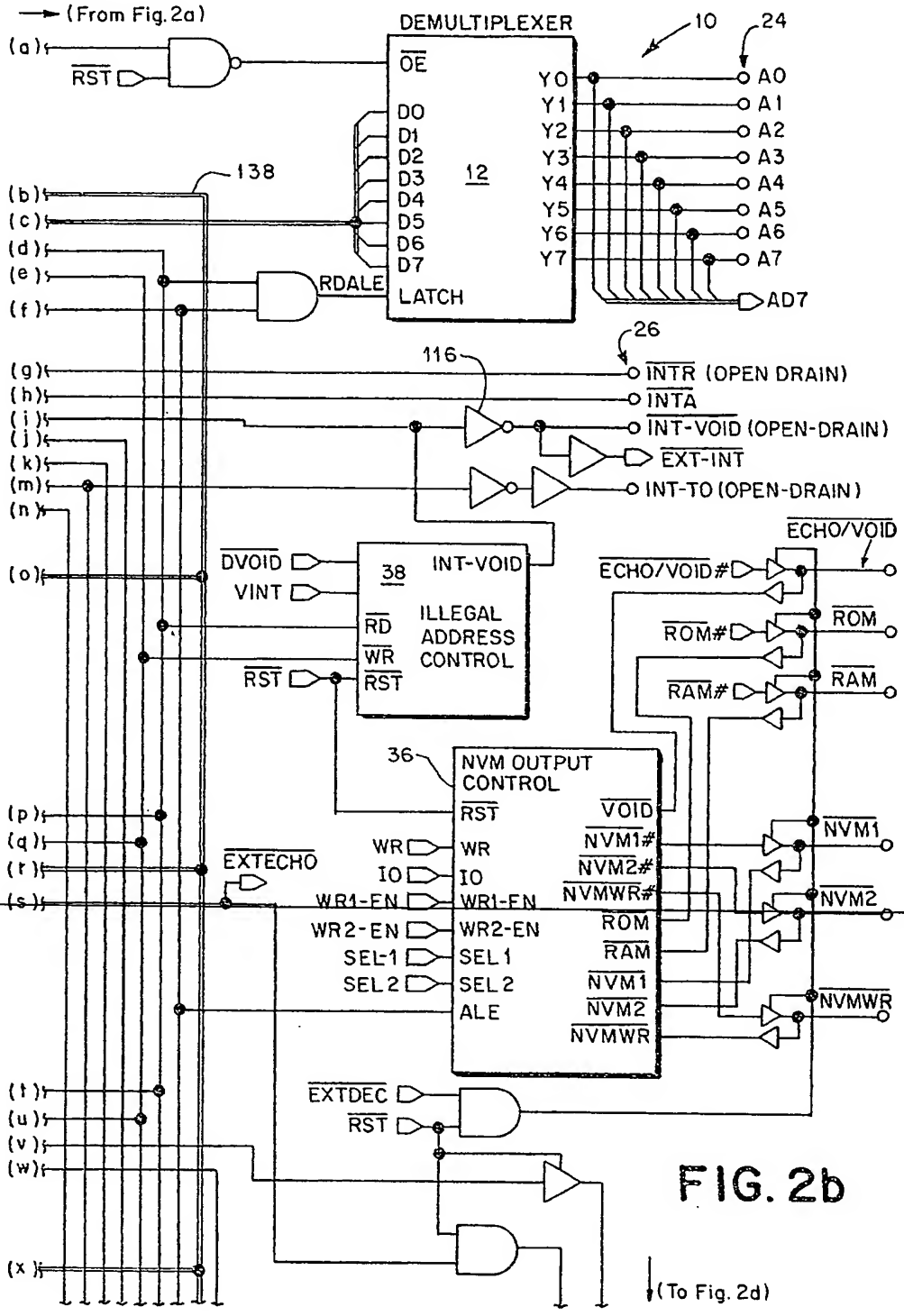
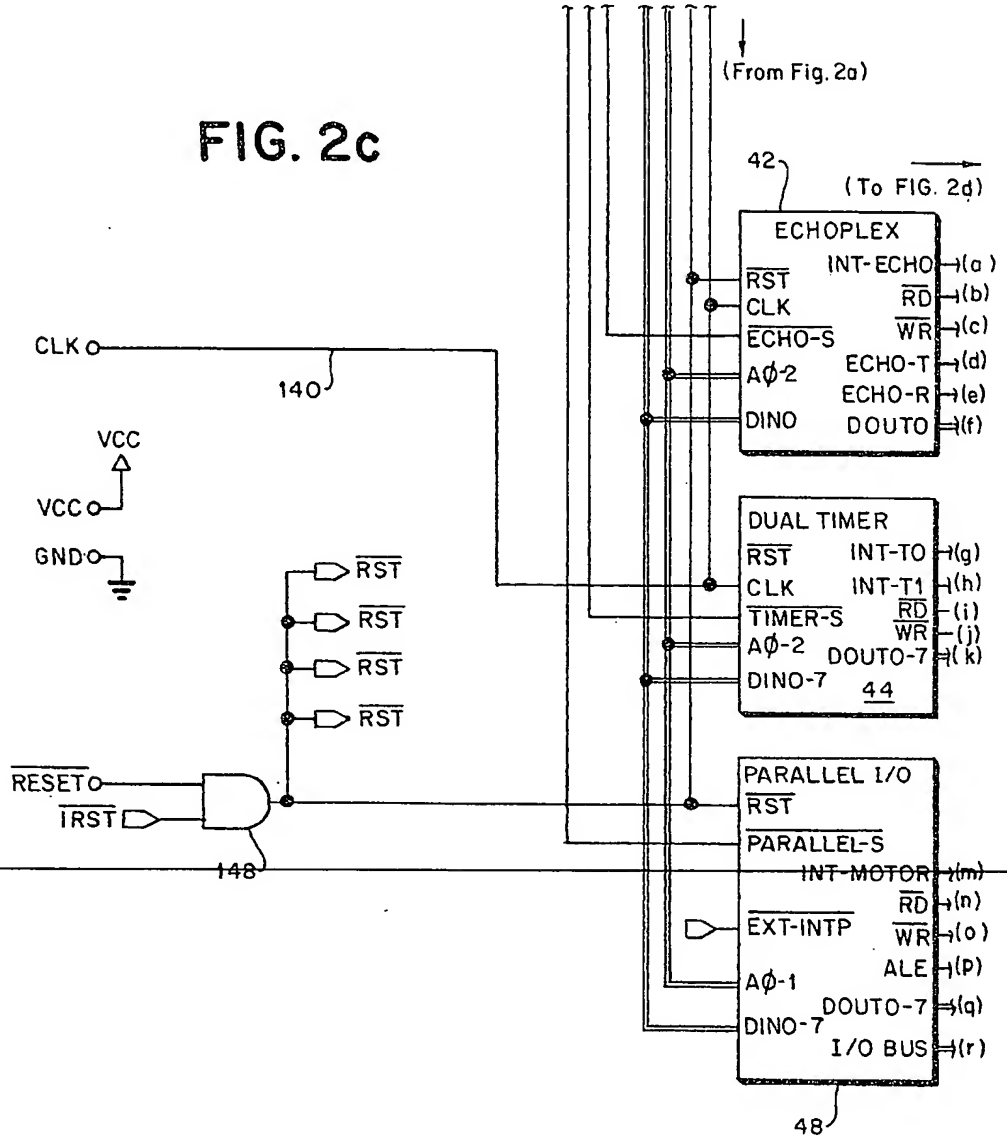

(From Fig. 2a)
DEMULTIPLEXER
10
24
OE
RST
D0
D1
D2
D3
D4
D5
D6
D7
12
LATCH
RDALE
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
A0
A1
A2
A3
A4
A5
A6
A7
AD7
138
26
116
INTR (OPEN DRAIN)
INTA
INT-VOID (OPEN-DRAIN)
EXT-INT
INT-TO (OPEN-DRAIN)
ECHO/VOID
ECHO/VOID#
DVOID
VINT
38
INT-VOID
ILLEGAL ADDRESS CONTROL
RD
WR
RST
ROM
ROM#
RAM
RAM#
36
NVM OUTPUT CONTROL
VOID
NVM1#
NVM2#
NVMWR#
ROM
RAM
NVM1
NVM2
NVMWR
EXTECHO
IO
WR1-EN
WR2-EN
SEL1
SEL2
ALE
EXTDEC
(To Fig. 2d)

FIG. 2b

FIG. 2c


(From Fig. 2a)
42
(To FIG. 2d)
ECHOPLEX
RST
CLK
ECHO-S
AΦ-2
DINO
INT-ECHO
RD
WR
ECHO-T
ECHO-R
DOUTO
(a)
(b)
(c)
(d)
(e)
(f)
CLK
140
VCC
VCC
GND
RST
RST
RST
RST
DUAL TIMER
RST
CLK
TIMER-S
AΦ-2
DINO-7
INT-TO
INT-T1
RD
WR
DOUTO-7
44
(g)
(h)
(i)
(j)
(k)
RESET
IRST
148
PARALLEL I/O
RST
PARALLEL-S
INT-MOTOR
RD
WR
EXT-INTP
ALE
AΦ-1
DOUTO-7
DINO-7
I/O BUS
(m)
(n)
(o)
(p)
(q)
(r)
48

1247252

21-5

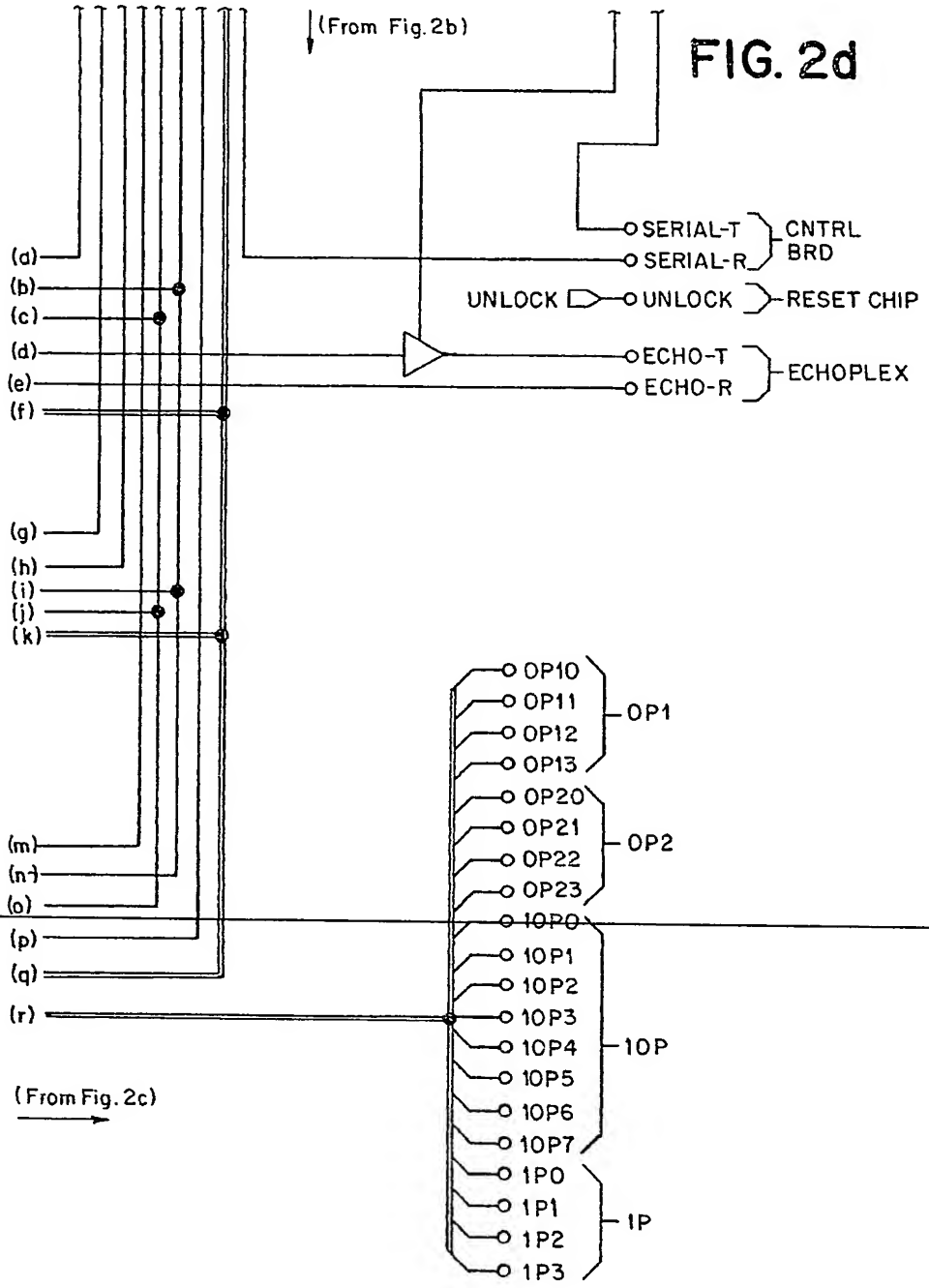
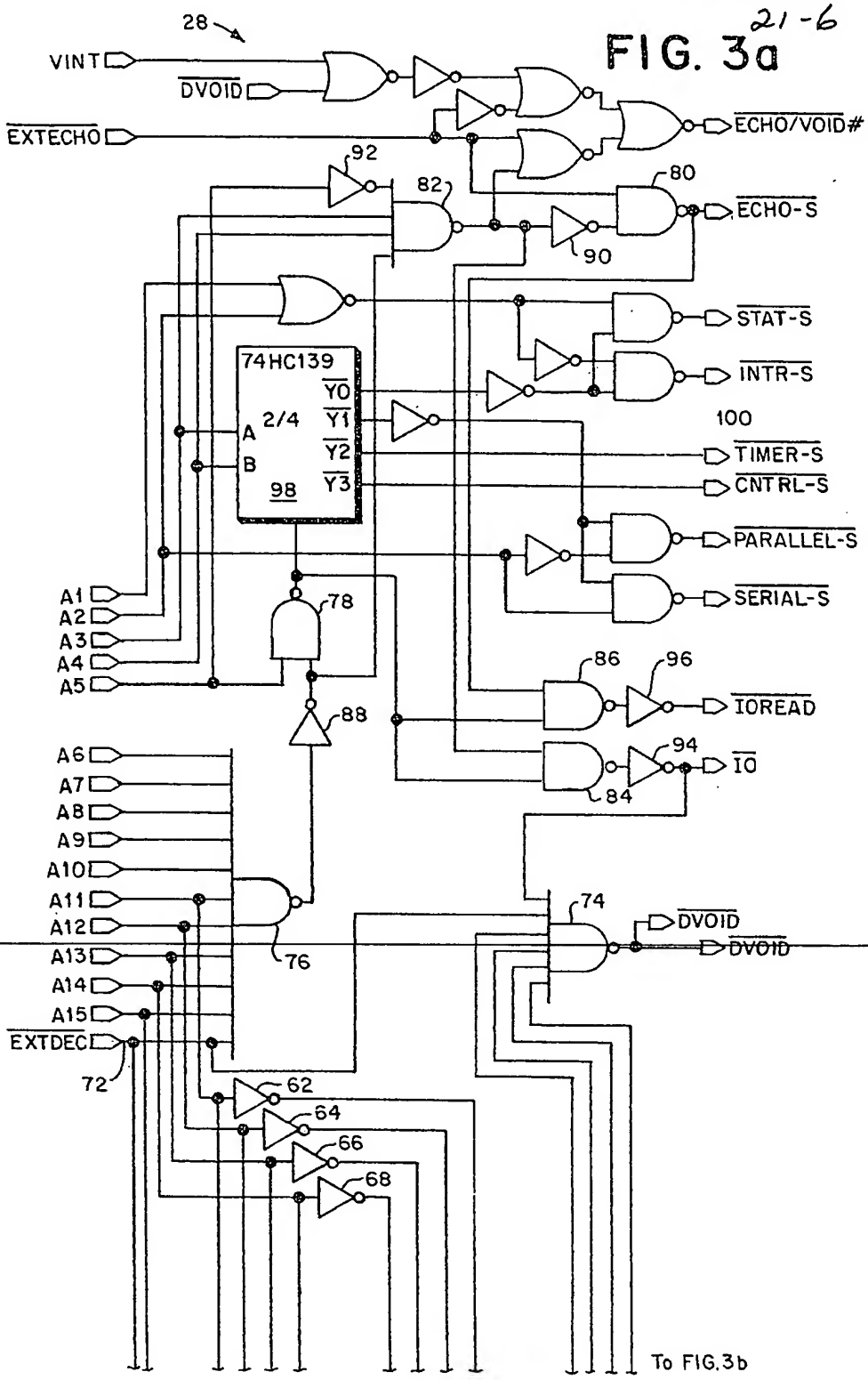
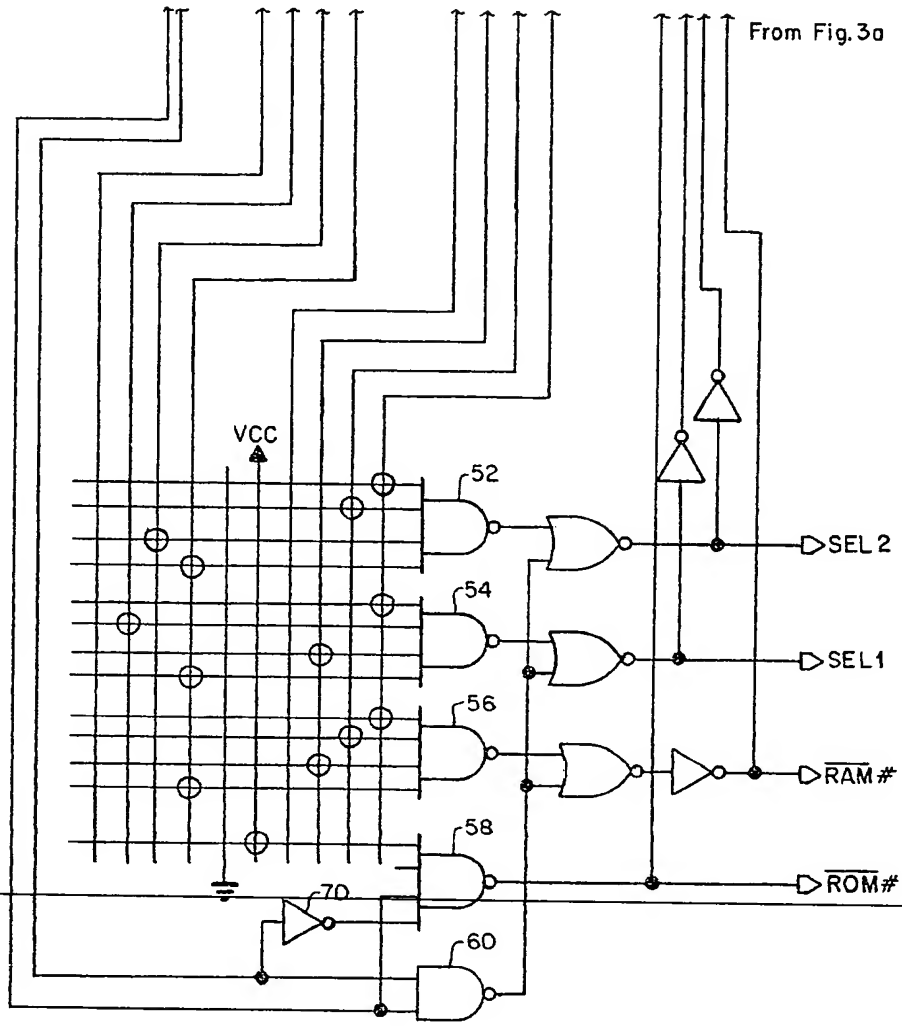


FIG. 2d

FIG. 3a


28
VINT
DVOID
EXTECHO
ECHO/VOID#
92
82
80
ECHO-S
90
STAT-S
INTR-S
74HC139
Y0
2/4
Y1
A
Y2
B
Y3
98
100
TIMER-S
CNTRL-S
PARALLEL-S
SERIAL-S
A1
A2
A3
A4
A5
78
86
96
IOREAD
88
94
IO
84
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
EXTDEC
72
76
74
DVOID
DVOID
62
64
66
68
To FIG.3b



⊕ INDICATES DEFAULT METALIZATION CONTACTS

FIG. 3b

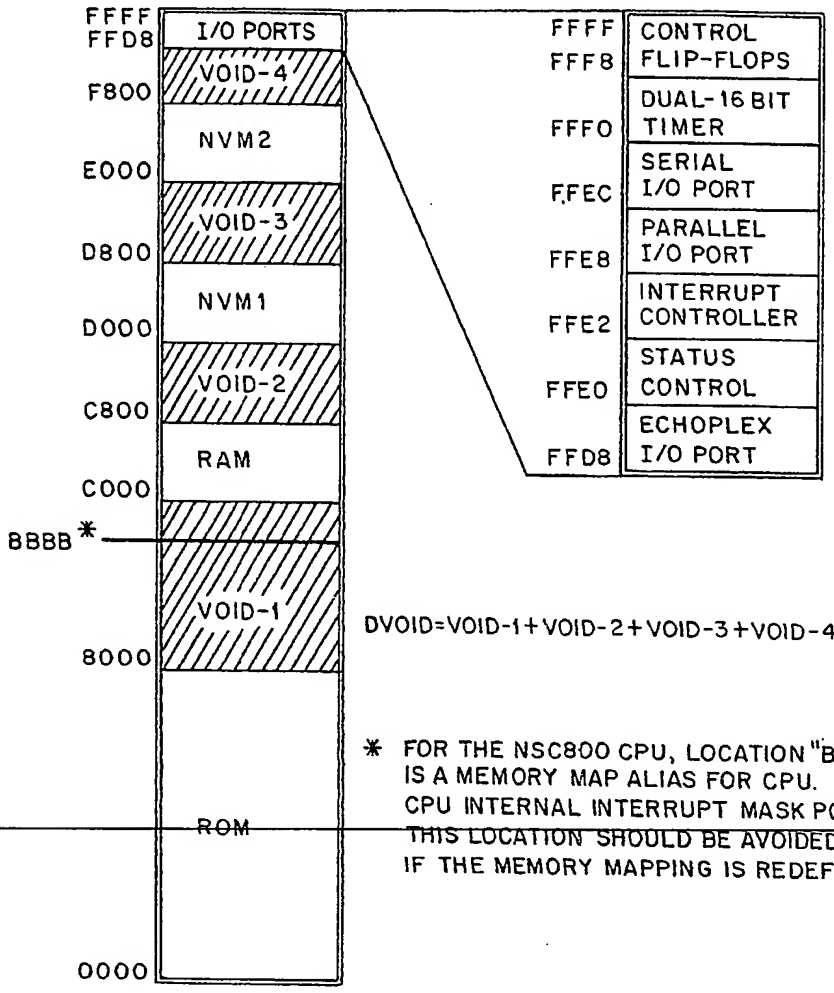

FFFF
FFD8
I/O PORTS
VOID-4
F800
NVM2
E000
VOID-3
D800
NVM1
D000
VOID-2
C800
RAM
C000
BBBB *
VOID-1
8000
ROM
0000
FFFF
FFF8
CONTROL FLIP-FLOPS
FFF0
DUAL-16 BIT TIMER
FFEC
SERIAL I/O PORT
FFE8
PARALLEL I/O PORT
FFE2
INTERRUPT CONTROLLER
FFE0
STATUS CONTROL
FFD8
ECHOPLEX I/O PORT
DVOID=VOID-1+VOID-2+VOID-3+VOID-4
* FOR THE NSC800 CPU, LOCATION "BBBB" IS A MEMORY MAP ALIAS FOR CPU. CPU INTERNAL INTERRUPT MASK PORT "BB". THIS LOCATION SHOULD BE AVOIDED EVEN IF THE MEMORY MAPPING IS REDEFINED.

FIG. 4

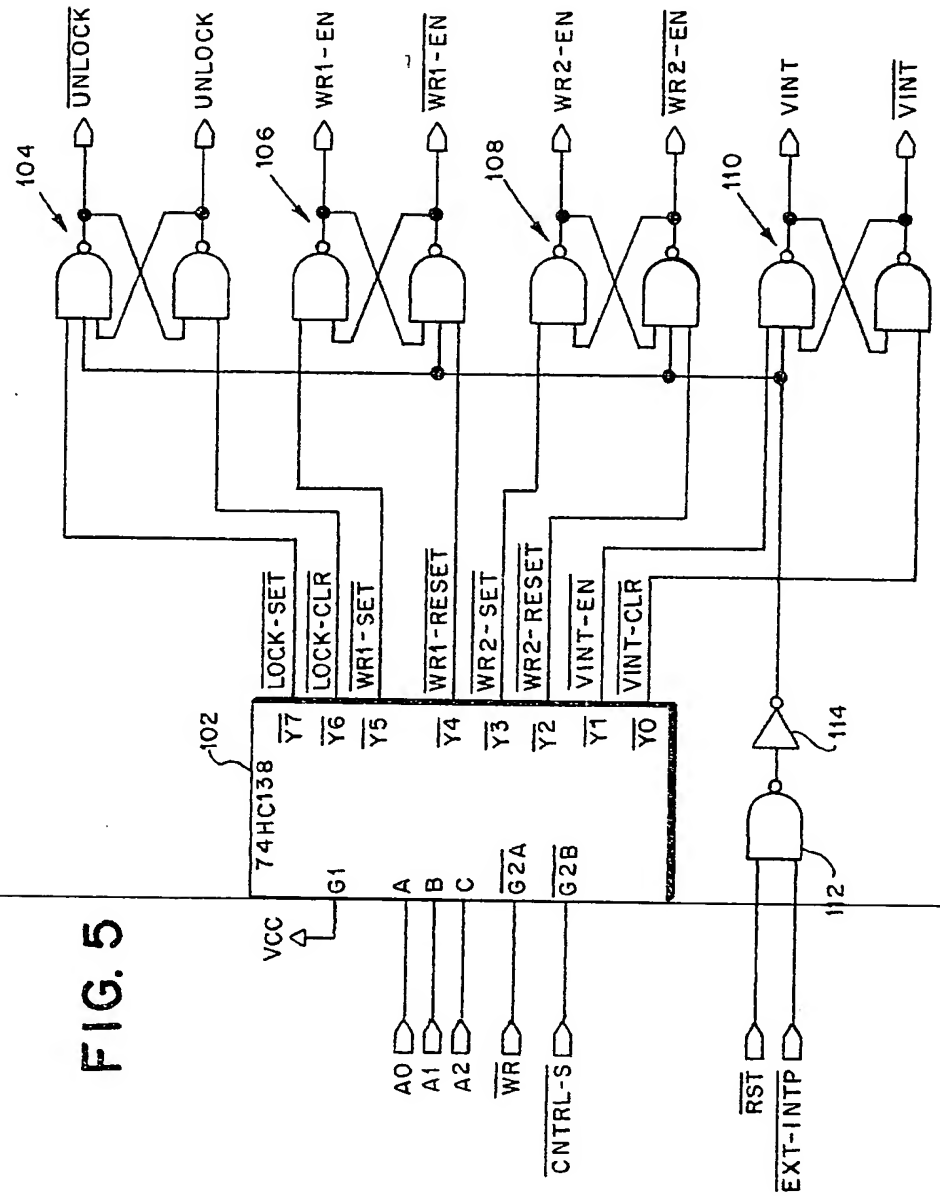

104
106
108
110
UNLOCK
UNLOCK
WR1-EN
WR1-EN
WR2-EN
WR2-EN
VINT
VINT
LOCK-SET
LOCK-CLR
WR1-SET
WR1-RESET
WR2-SET
WR2-RESET
VINT-EN
VINT-CLR
102
74HC138
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
G1
A
B
C
G2A
G2B
114
112
VCC
A0
A1
A2
WR
CNTRL-S
RST
EXT-INTP

FIG. 5

1247252

21-10

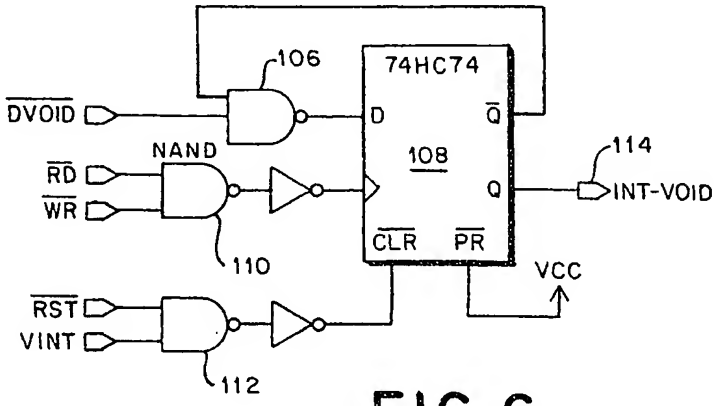
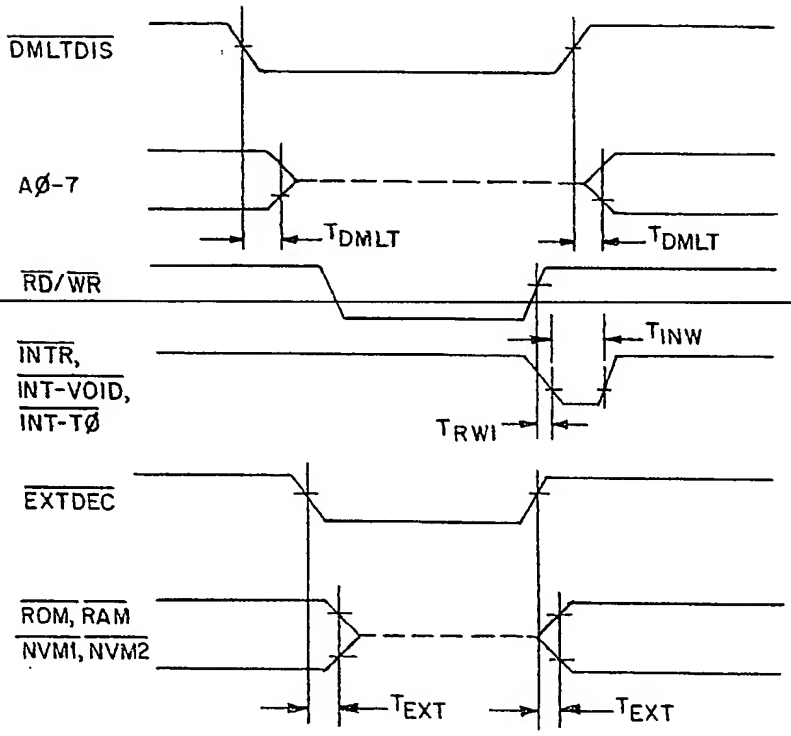


FIG. 6

FIG. 11



Sam E. Mc Burney

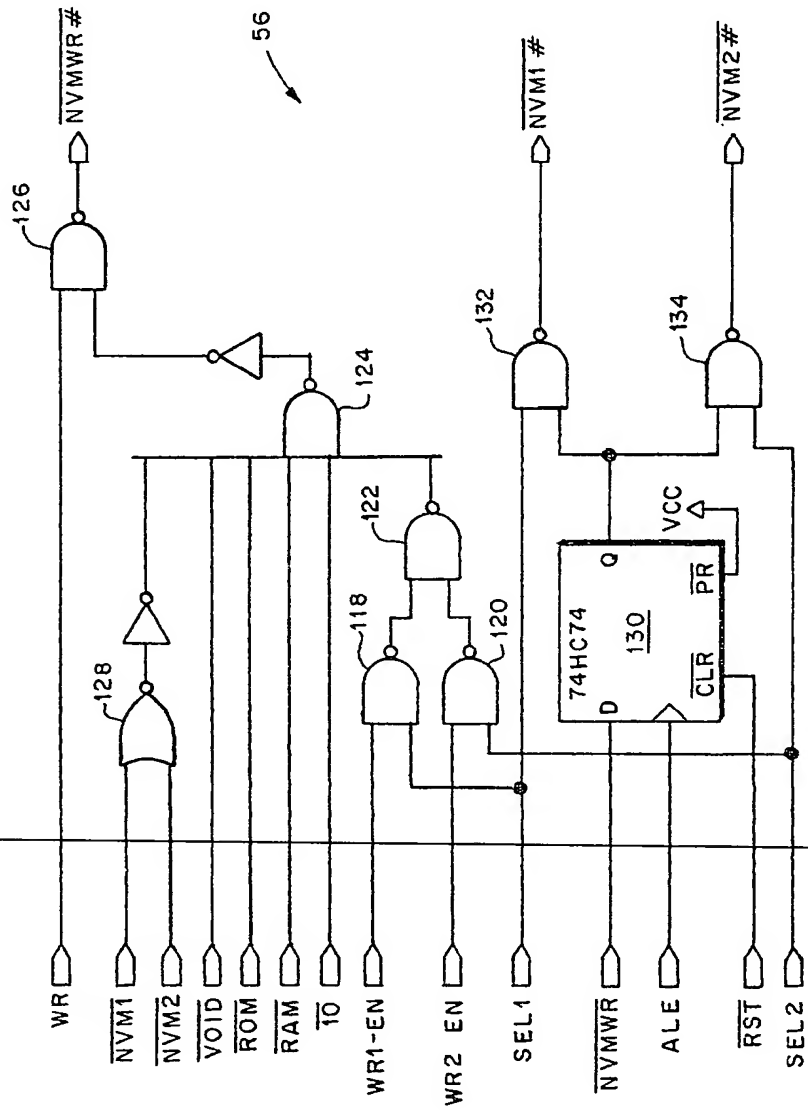
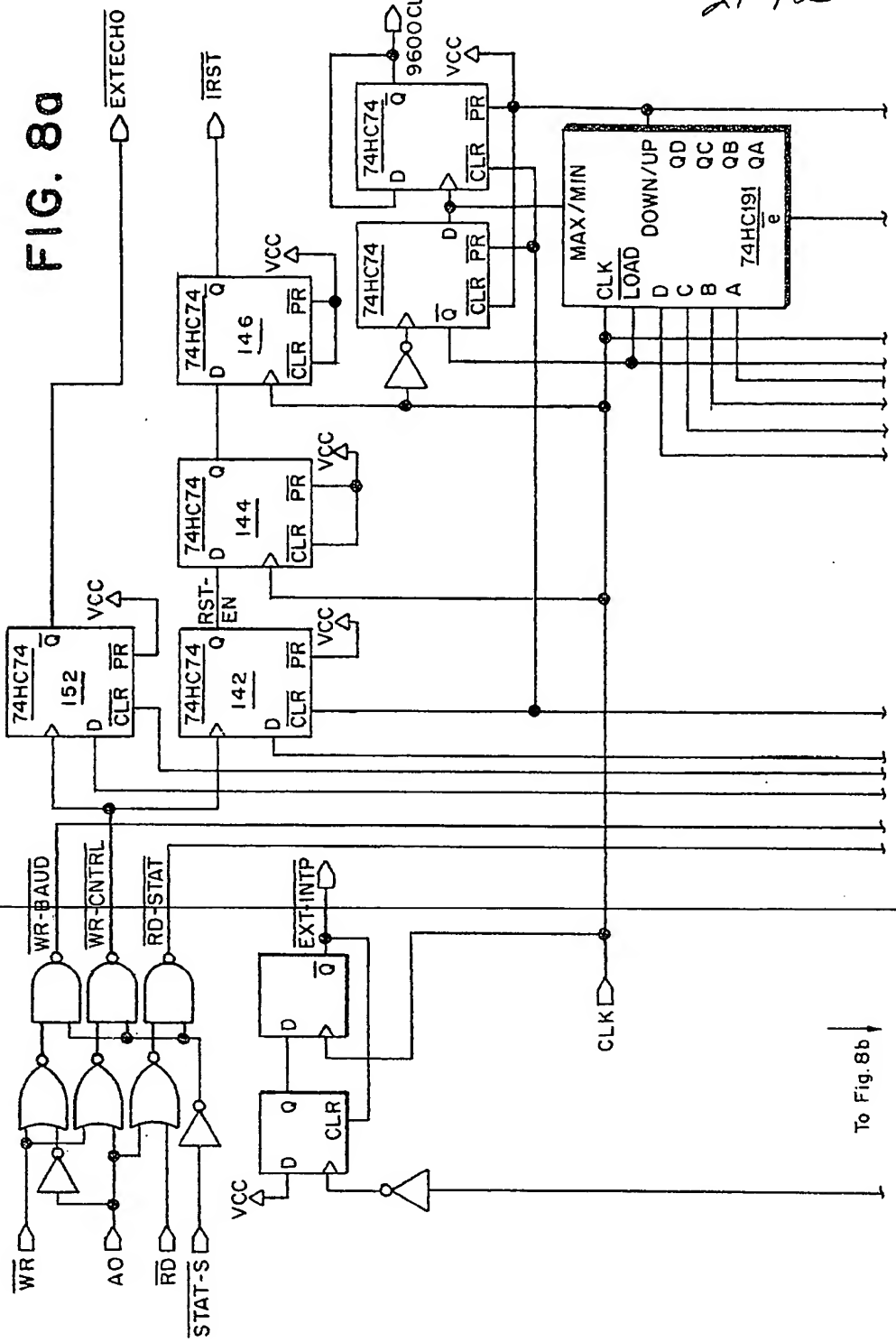

56
NVMWR#
126
124
132
NVM1#
134
NVM2#
122
VCC
Q
PR
74HC74
130
CLR
D
118
120
128
WR
NVM1
NVM2
VOID
ROM
RAM
IO
WR1-EN
WR2 EN
SEL1
NVMWR
ALE
RST
SEL2

FIG. 7

1247252
21-12

FIG. 8a



1247252
21-13

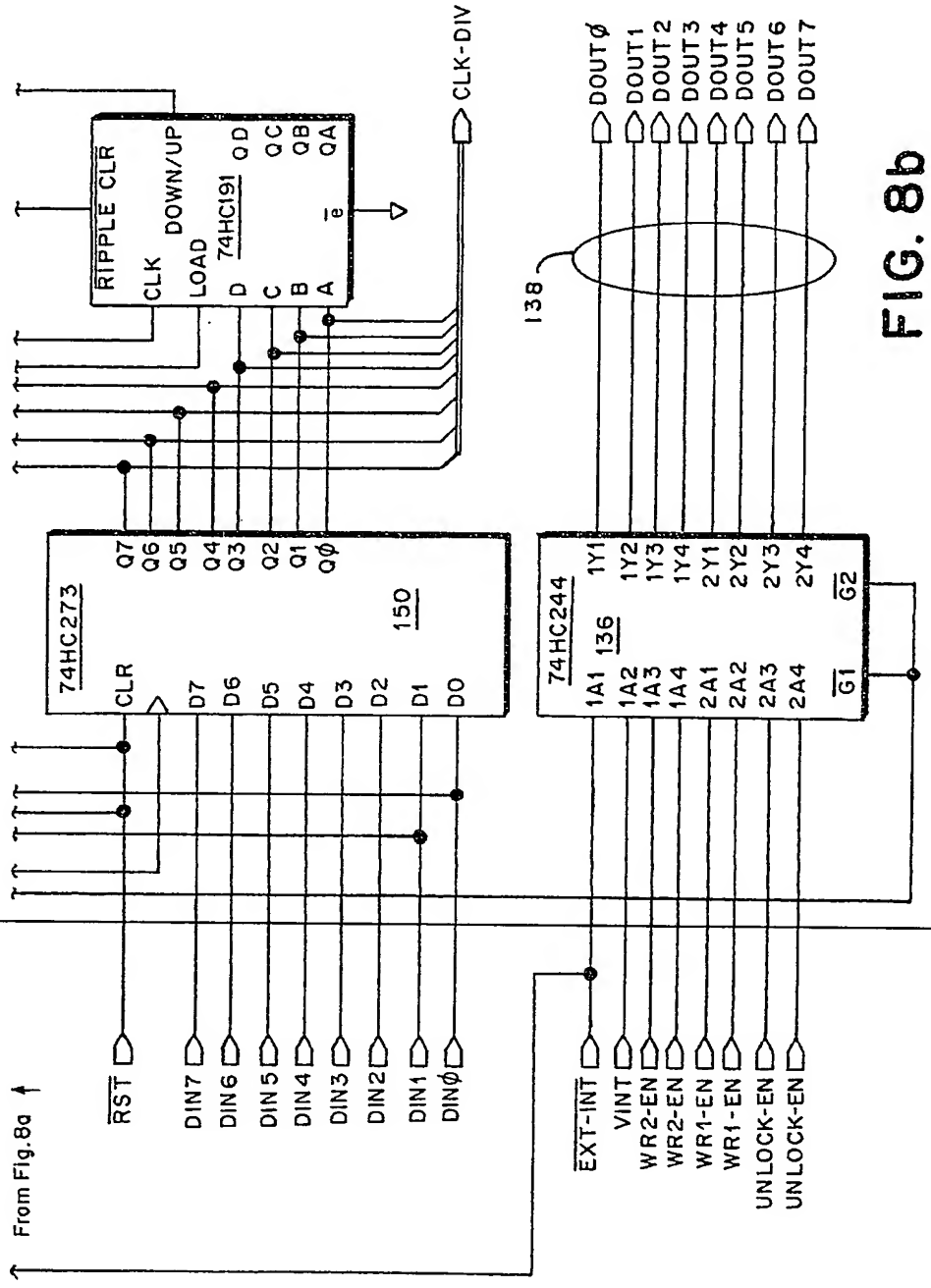
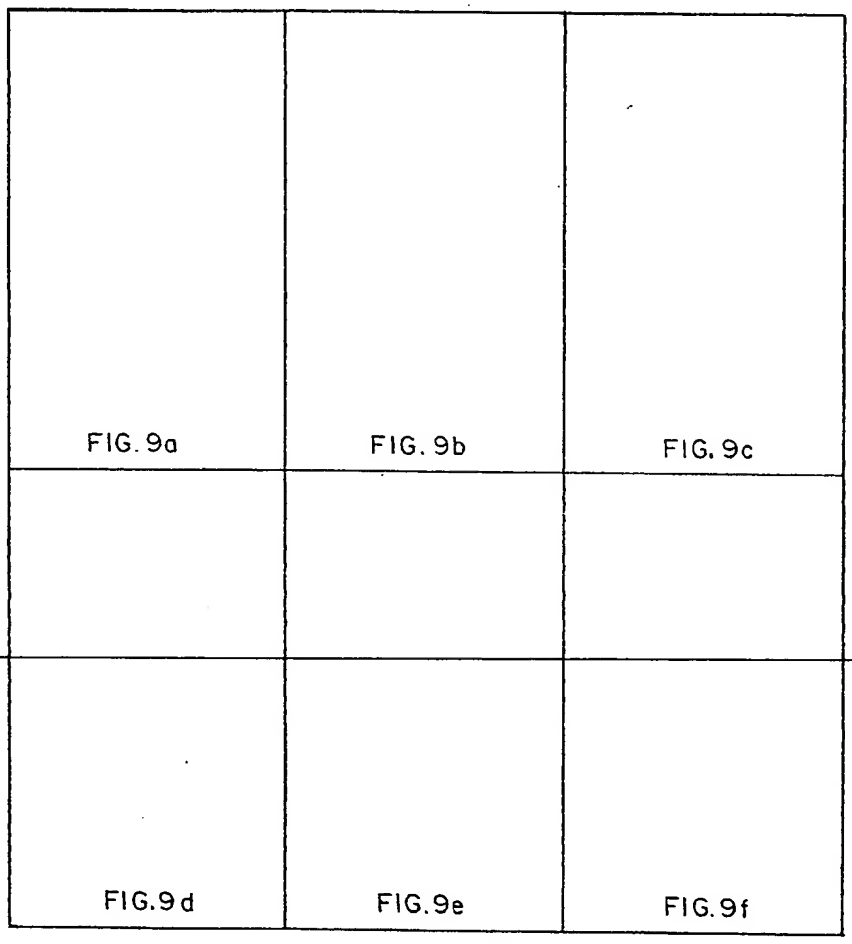


FIG. 8b

Sid H. Bennett

1247252
21-14

FIG. 9



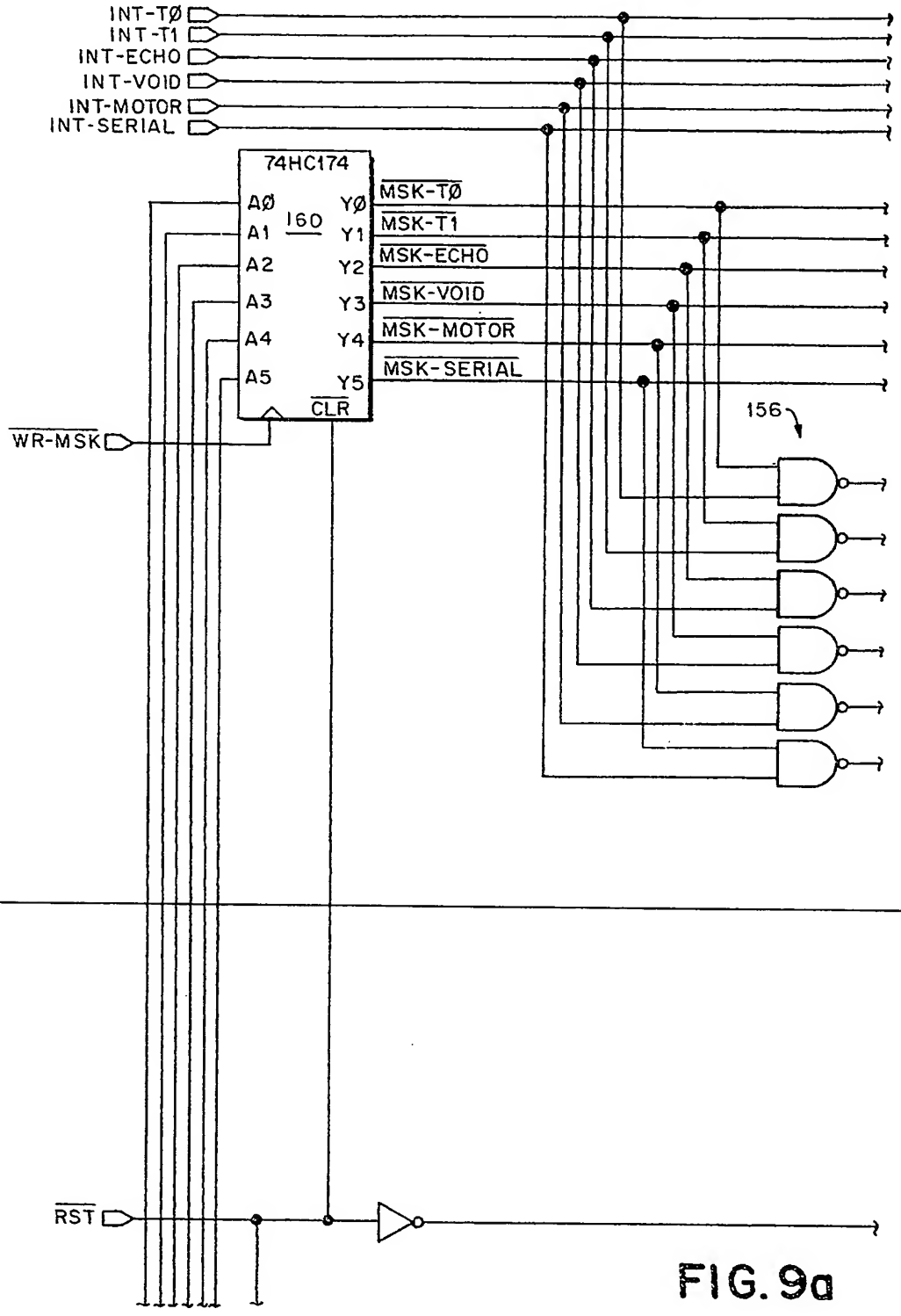


FIG. 9a

Sincerely yours,

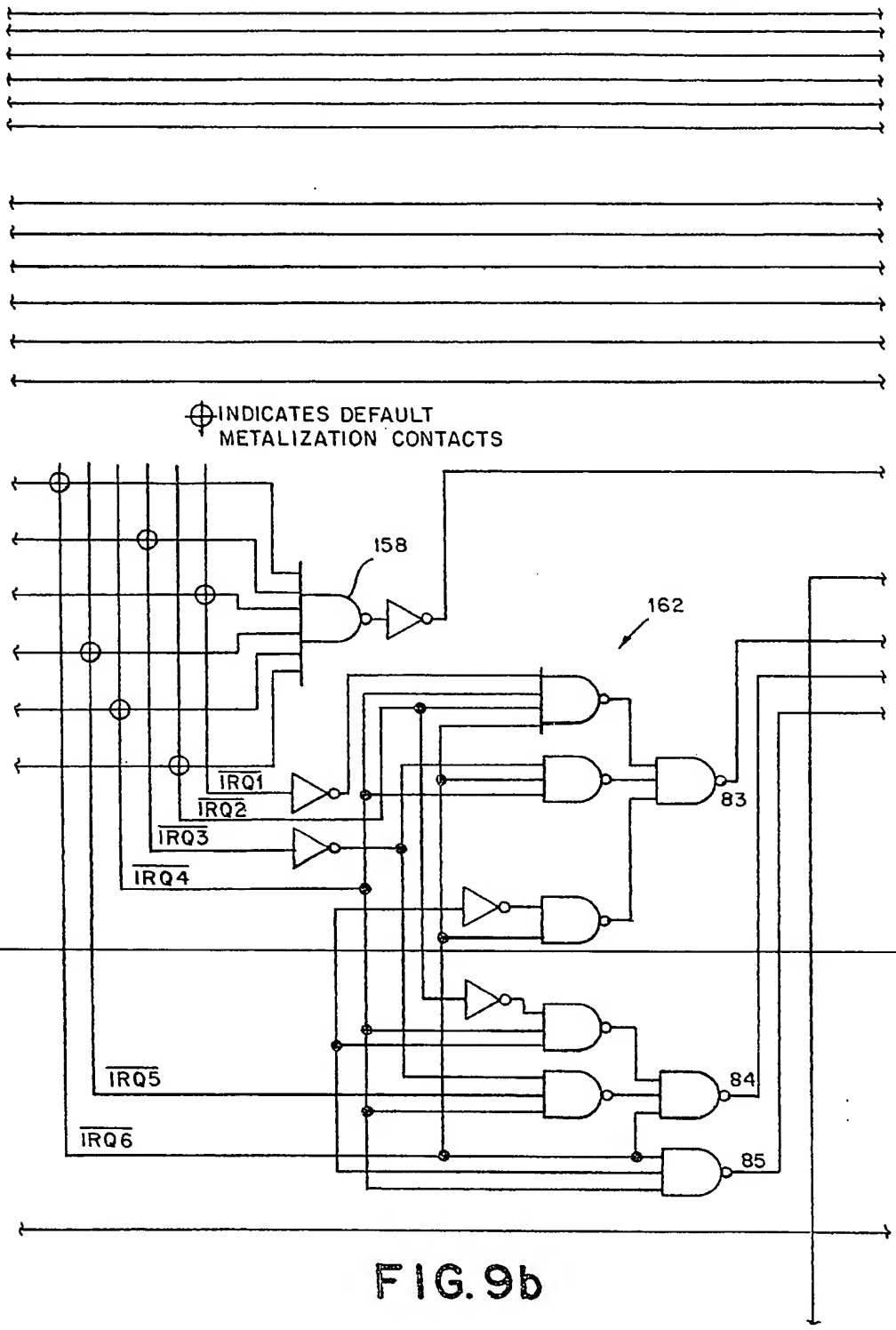

INDICATES DEFAULT
METALIZATION CONTACTS
158
162
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
83
84
85

FIG. 9b

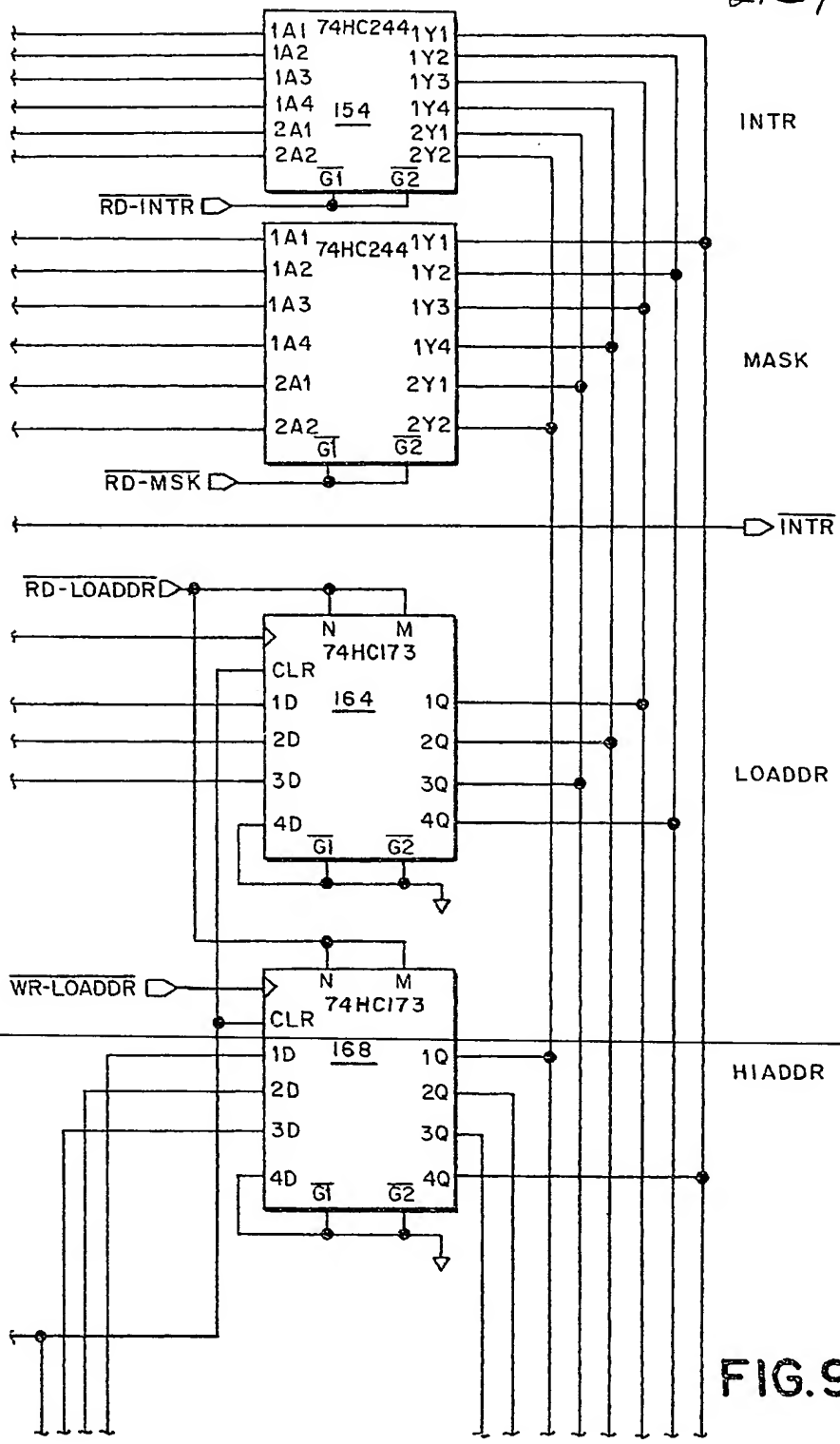

74HC244
154
1A1
1A2
1A3
1A4
2A1
2A2
G1
G2
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
INTR
RD-INTR
74HC244
MASK
RD-MSK
INTR
RD-LOADDR
74HC173
164
N
M
CLR
1D
2D
3D
4D
1Q
2Q
3Q
4Q
LOADDR
WR-LOADDR
74HC173
168
HIADDR

FIG.9c

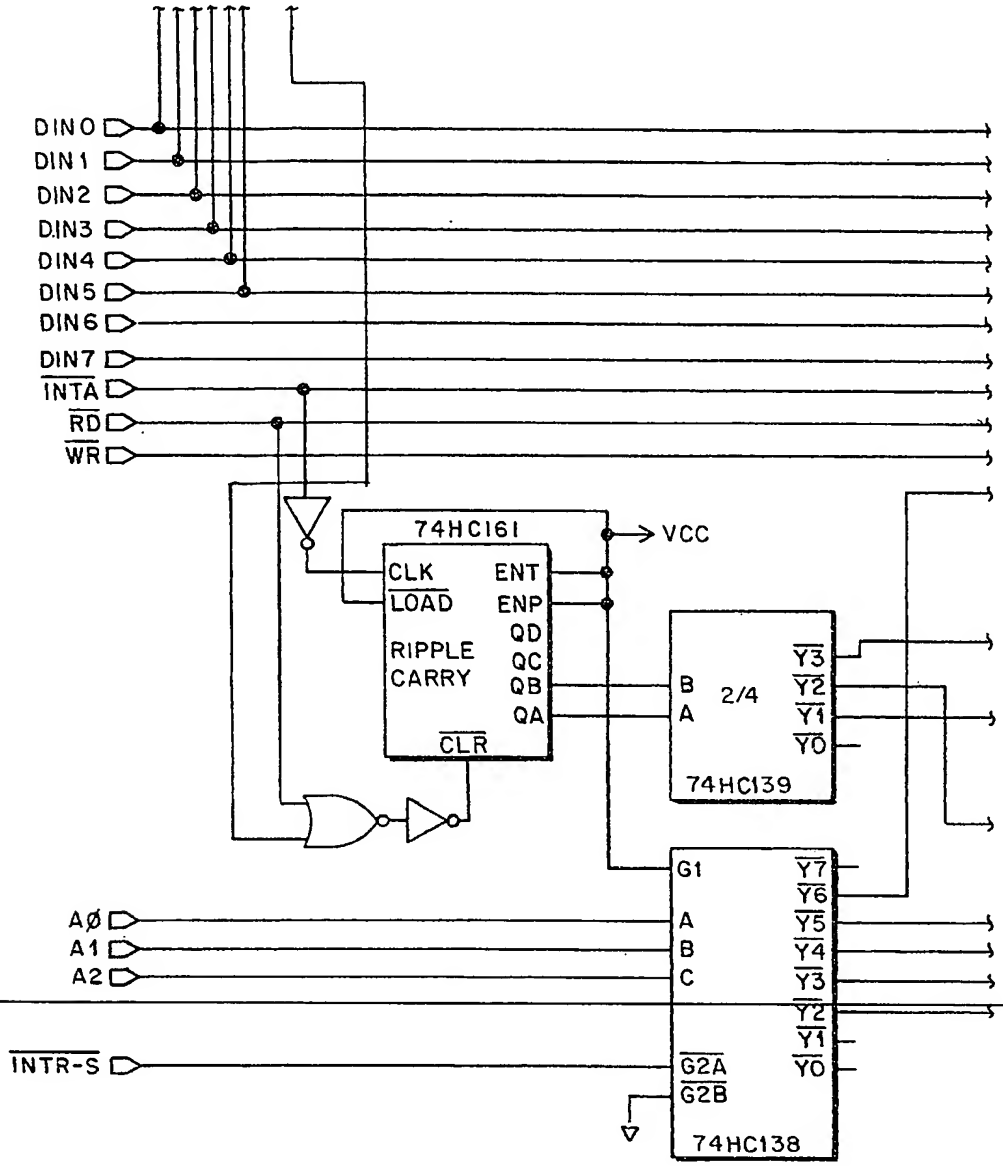

DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
INTA
RD
WR
74HC161
VCC
CLK
LOAD
ENT
ENP
QD
QC
QB
QA
RIPPLE
CARRY
CLR
B
A
2/4
Y3
Y2
Y1
Y0
74HC139
G1
A
B
C
G2A
G2B
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
74HC138
AØ
A1
A2
INTR-S

FIG. 9d

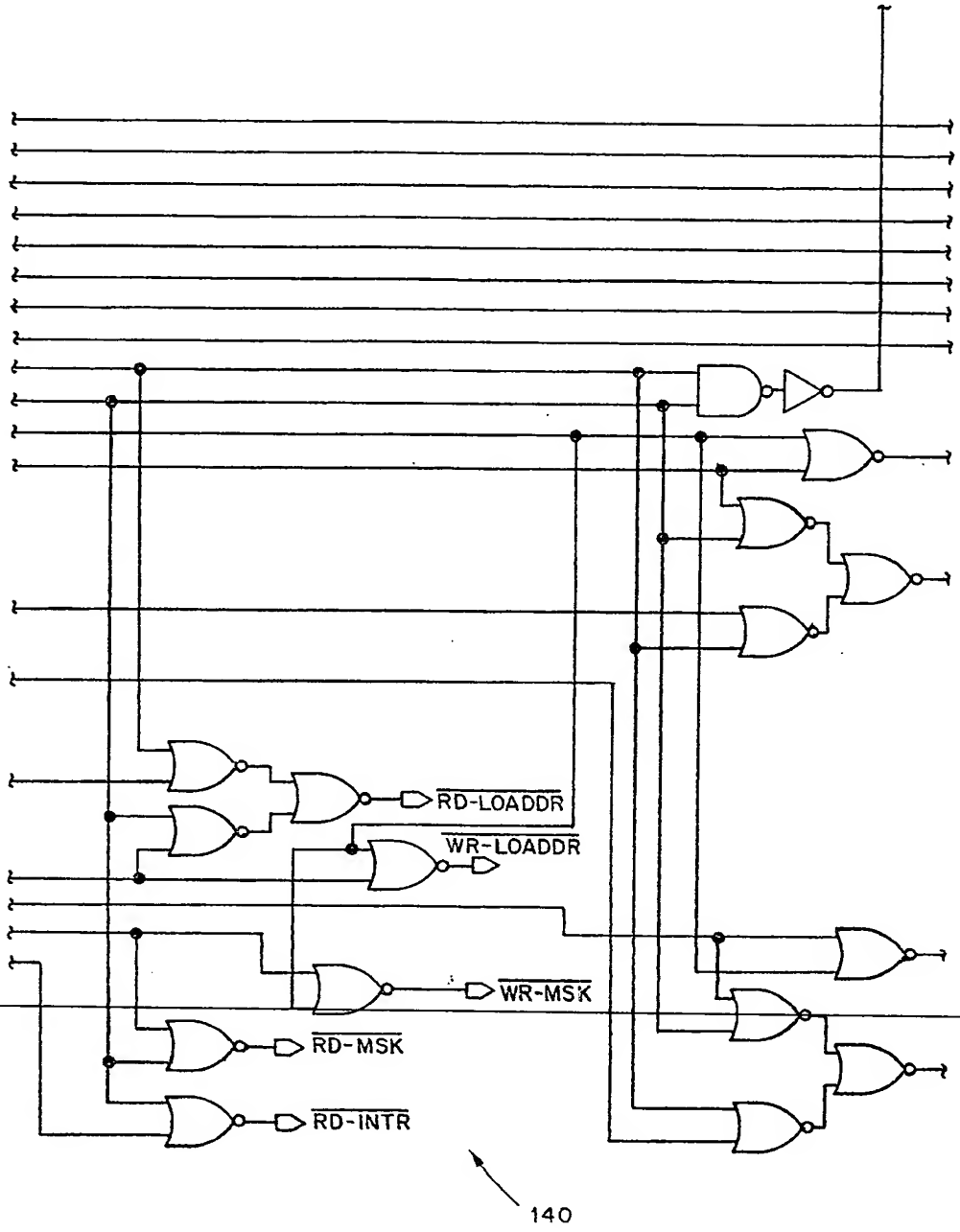


FIG. 9e

1247252

21-20

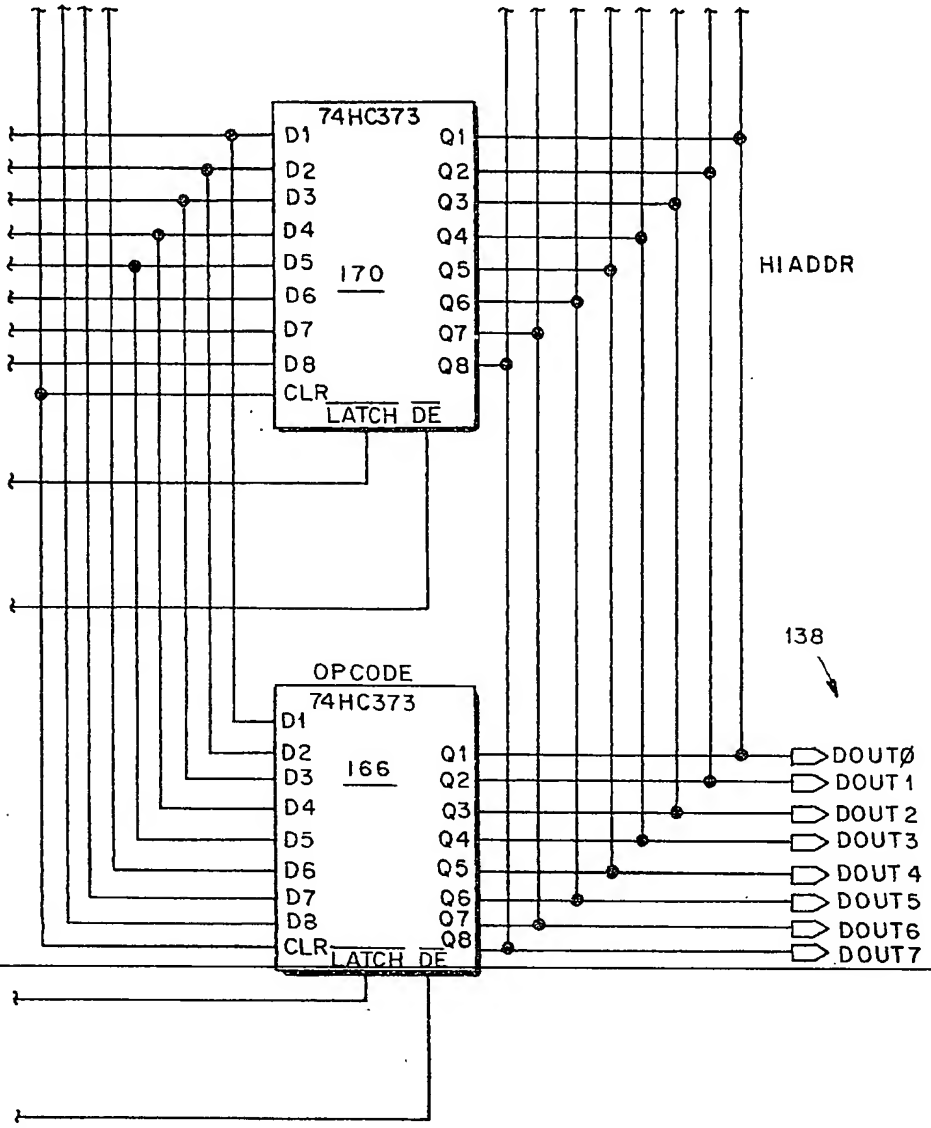


FIG. 9f

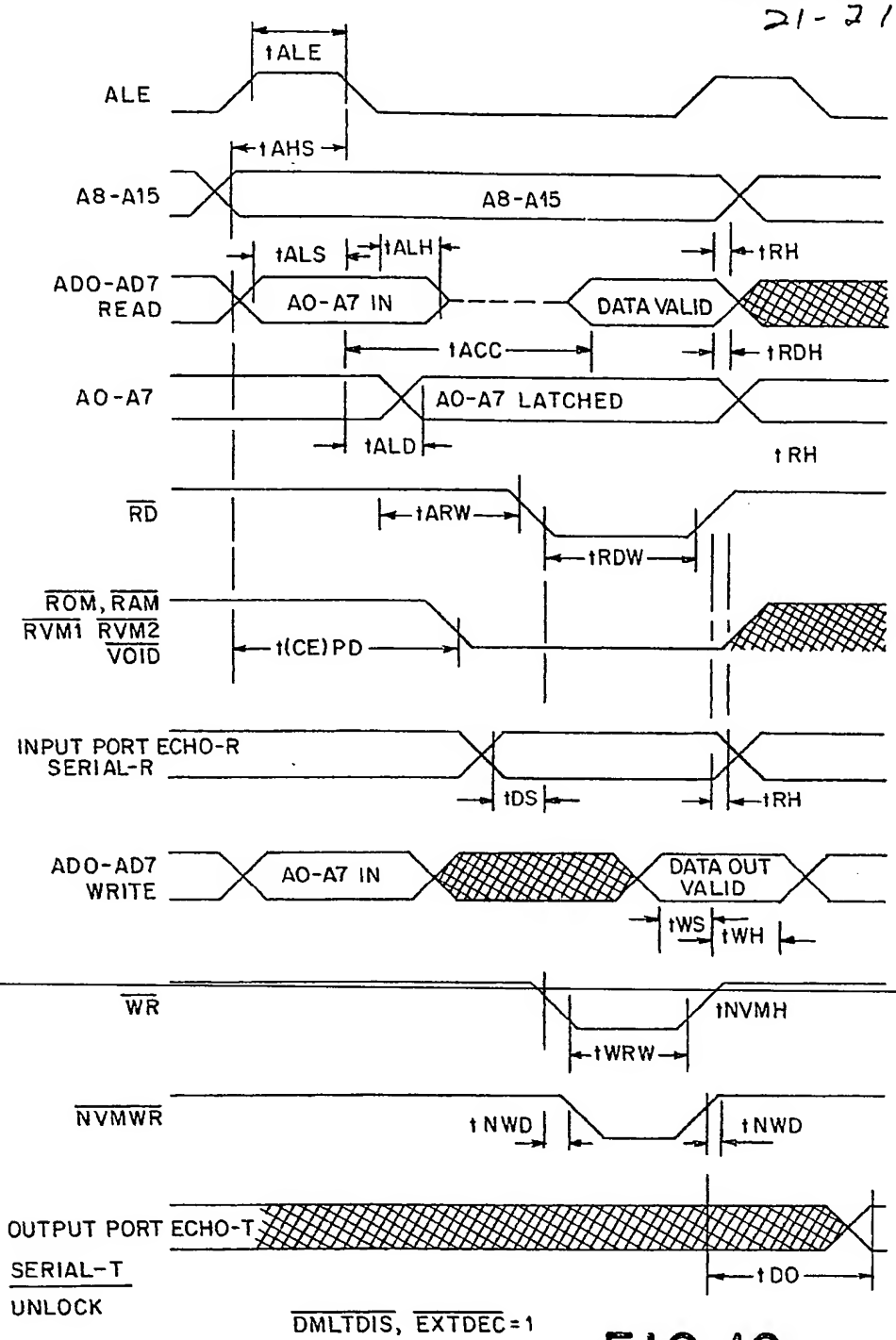

tALE
ALE
tAHS
A8-A15
A8-A15
tALS
tALH
tRH
AD0-AD7
READ
A0-A7 IN
DATA VALID
tACC
tRDH
A0-A7
A0-A7 LATCHED
tALD
tRH
RD
tARW
tRDW
ROM, RAM
RVM1 RVM2
VOID
t(CE)PD
INPUT PORT ECHO-R
SERIAL-R
tDS
tRH
AD0-AD7
WRITE
A0-A7 IN
DATA OUT
VALID
tWS
tWH
WR
tNVMH
tWRW
NVMWR
tNWD
tNWD
OUTPUT PORT ECHO-T
SERIAL-T
UNLOCK
tDO
DMLTDIS, EXTDEC=1

FIG. 10

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☑ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.

THIS PAGE BLANK (USPTO)